m

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_06818

# MODEL
# 373XXA
# VECTOR NETWORK ANALYZER

# MAINTENANCE MANUAL

Anritsu

490 JARVIS DRIVE | MORGAN HILL, CA 95037-2809

P/N: 10410-00185
REVISION: D
PRINTED: MARCH 2000
COPYRIGHT 1996 ANRITSU CO.

## WARRANTY

The ANRITSU product(s) listed on the title page is (are) warranted against defects in materials and workmanship for one year from the date of shipment.
ANRITSU's obligation covers repairing or replacing products which prove to be defective during the warranty period. Buyers shall prepay transportation charges for equipment returned to ANRITSU for warranty repairs. Obligation is limited to the original purchaser. ANRITSU is not liable for consequential damages.

## LIMITATION OF WARRANTY

The foregoing warranty does not apply to ANRITSU connectors that have failed due to normal wear. Also, the warranty does not apply to defects resulting from improper or inadequate maintenance by the Buyer, unauthorized modification or misuse, or operation outside of the environmental specifications of the product. No other warranty is expressed or implied, and the remedies provided herein are the Buyer's sole and exclusive remedies.

## TRADEMARK ACKNOWLEDGEMENTS

V Connector and K Connector are registered trademarks of ANRITSU Company.
ANACAT is a registered trademark of EEsof, Inc.
Ink Jet and Think Jet are registered trademarks of Hewlett-Packard Co.
MS-DOS is a registered trademark of Microsoft Corporation.

## NOTICE

ANRITSU Company has prepared this manual for use by ANRITSU Company personnel and customers as a guide for the proper installation, operation and maintenance of ANRITSU Company equipment and computer programs. The drawings, specifications, and information contained herein are the property of ANRITSU Company, and any unauthorized use or disclosure of these drawings, specifications, and information is prohibited; they shall not be reproduced, copied, or used in whole or in part as the basis for manufacture or sale of the equipment or software programs without the prior written consent of ANRITSU Company.

# DECLARATION OF CONFORMITY

**Manufacturer's Name:** ANRITSU COMPANY

**Manufacturer's Address:** Microwave Measurements Division
490 Jarvis Drive
Morgan Hill, CA 95037-2809
USA

declares that the product specified below:

**Product Name:** Microwave Vector Network Analyzers

**Model Number:** 371XXA, 372XXA, 372XXB, 373XXA

conforms to the requirement of:

EMC Directive 89/336/EEC as amended by Council Directive 92/31/EEC & 93/68/EEC
Low Voltage Directive 73/23/EEC as amended by Council directive 93/68/EEC

**Electromagnetic Interference:**

| | |
|---|---|
| Emissions: | CISPR 11:1990/EN55011:1991 Group 1 Class A |
| Immunity: | IEC 1000-4-2:1995/prEN50082-1:1995 - 4kV CD, 8kV AD<br>IEC 1000-4-3:1993/ENV50140:1994 - 3V/m<br>IEC 1000-4-4:1995/prEN50082-1:1995 - 0.5kV SL, 1kV PL<br>IEC 1000-4-5:1995/prEN50082-1:1995 - 0.5kV - 1kV LN<br>0.5kV - 1kV NG<br>0.5kV - 1kV GL |

**Electrical Safety Requirement:**

| | |
|---|---|
| Product Safety: | IEC 1010-1:1990 + A1/EN61010-1:1993 |

Jeri Blasi
Manager of Corporate Quality

Morgan Hill, CA

5-SEPT-97
Date

European Contact: For Anritsu product EMC & LVD information, contact Anritsu LTD, Rutherford Close, Stevenage Herts, SG1 2EF UK, (FAX 44-1438-740202)

# *Table of Contents, Narrative*

**Chapter 1 — General Service Information**
This chapter provides a general description of Series373XXA Vector Network Analyzer systems, system serial numbers, and frequency ranges. It explains the level of maintenance covered in this manual and the service strategy used throughout this manual. It also contains static-sensitive component handling precautions and a list of recommended test equipment.

**Chapter 2 — Replaceable Parts**
This chapter lists all replaceable subassemblies and components for all373XXA models. It explains the ANRITSUexchange assembly program and provides parts ordering information.

**Chapter 3 — Operational Tests**
This chapter contains procedures that provide a means of fully testing the373XXA VNA system for proper operation and signal stability. These tests are intended to be used as a periodic check of the operational functionality of the373XXA.

**Chapter 4 — Performance Verification Procedures**
This chapter provides detailed procedures for verifying that the performance of the373XXA meets minimum performance standards.

**Chapter 5 — Troubleshooting**
This chapter provides information for troubleshooting Series373XXA Vector Network Analyzer systems. The troubleshooting procedures contained in this chapter support fault isolation down to a replaceable subassembly.

**Chapter 6 — Adjustments**
This chapter provides adjustment procedures for all models of Series373XXA Vector Network Analyzer systems. These procedures are used after replacement or repair of one or more critical subassemblies, or as indicated by the Performance Verification Procedures contained in Chapter 4.

**Chapter 7 — System Description**
This chapter provides descriptions of the functional operation of the major assemblies contained in Series373XXA Vector Network Analyzer systems. The operation of all major circuit blocks is described so that the reader may better understand the function of each assembly as part of the overall operation.

**Chapter 8— Removal and Replacement Procedures**
This chapter describes how to gain access to all of the major assemblies and major parts for ¬troubleshooting and/or replacement.

**Appendix A — Diagnostic Menus**
This appendix contains descriptions and usage information for the Diagnostic Menus that are available via the front panel Option Menu key.

**Appendix B — Error Codes/Messages**
This appendix contains a listing of the Error Codes/Messages. Also included is a description of the information fields that are part of the error messages.

**Appendix C — Connector Maintenance Check Procedures**

This appendix contains procedures and information needed to perform maintenance checks (including pin-depth measurements) for the connectors on all ANRITSU supplied Calibration/Verification Kit components, Through-cables, and other associated RF/microwave components.

**Appendix D — Performance Specifications**

**Appendix E — Verification Software Users Guide**

This appendix contains the Model 360X/372XXB VNA Performance Verification Software Users Guide, P/N: 10410-00208. This Software Users Guide explains in detail the procedures to be used for the installation and operation of the 373XXA VNA Verification Software on your computer/controller.

**Index**

# *Chapter 1*
# *General Information*

## *Table of Contents*


| | | |
|---|---|---|
| 1-1 | SCOPE OF MANUAL | 1-3 |
| 1-2 | INTRODUCTION | 1-3 |
| 1-3 | IDENTIFICATION NUMBER | 1-3 |
| 1-4 | ONLINE MANUAL | 1-3 |
| 1-5 | SYSTEM DESCRIPTION | 1-4 |
| 1-6 | RELATED MANUALS | 1-4 |
| 1-7 | STANDARD OPTIONS | 1-4 |
| 1-8 | SERVICE STRATEGY | 1-5 |
| | Functional Assembly Level Troubleshooting | 1-5 |
| | Internal Hardware Adjustments and Calibrations | 1-5 |
| | Internal Service Log | 1-5 |
| | System Test/Certification | 1-6 |
| | Preventive Service | 1-6 |
| | Servicing Specially Modified Instruments | 1-6 |
| 1-9 | SERVICE SUPPORT | 1-6 |
| | Technical Support | 1-7 |
| | Field Service Kits | 1-7 |
| | Service Software | 1-7 |
| | Verification Kits | 1-8 |
| | Test Fixtures/ Aids | 1-8 |
| | Failed Assembly Exchange Program | 1-8 |
| 1-10 | PERFORMANCE SPECIFICATIONS | 1-9 |
| 1-11 | SERVICE CENTERS | 1-9 |
| 1-12 | STATIC SENSITIVE COMPONENT HANDLING PROCEDURES | 1-9 |
| 1-13 | RECOMMENDED TEST EQUIPMENT | 1-9 |

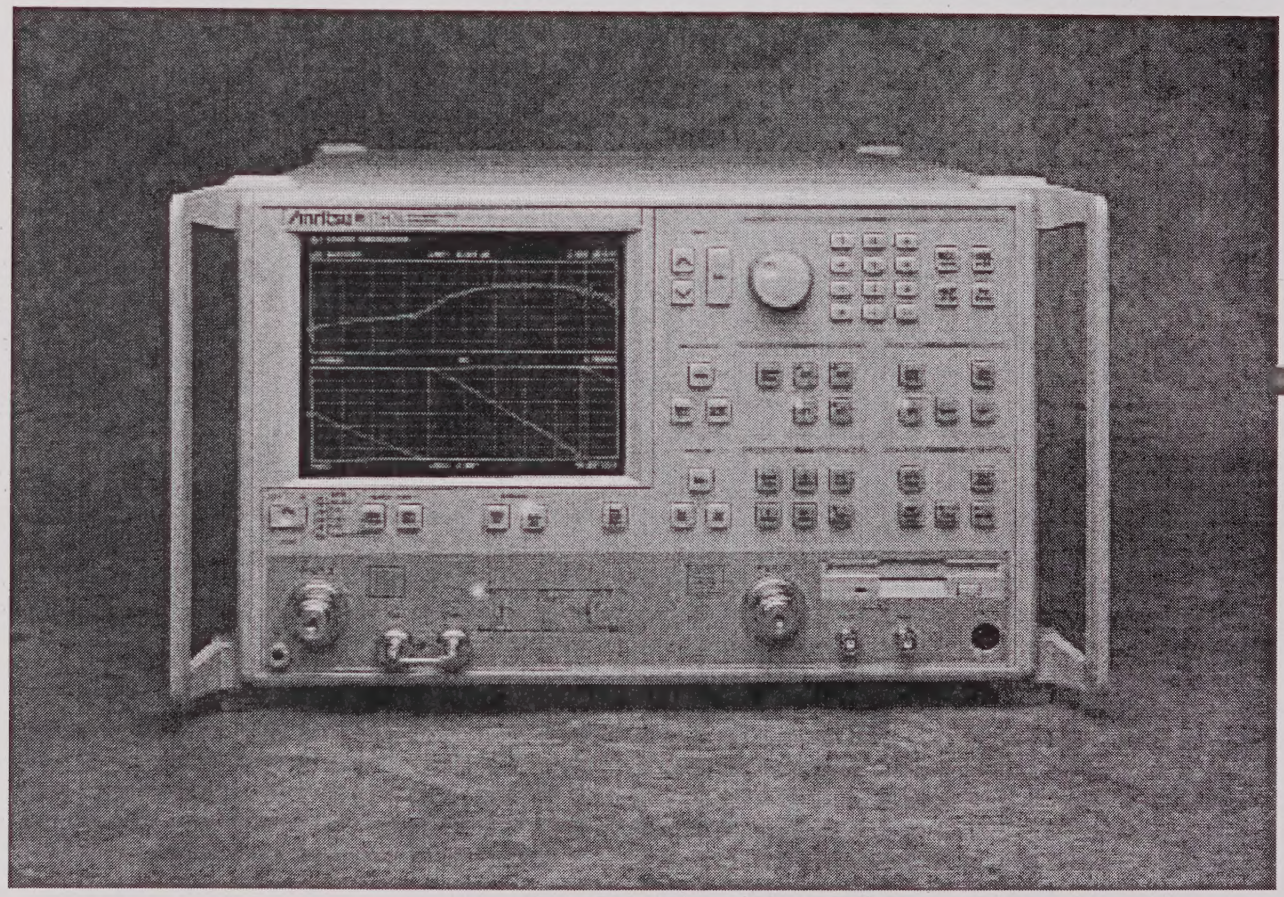



**Figure 1-1.** *Series 373XXA Vector Network Analyzer System*

# Chapter 1
# General Information

## 1-1 SCOPE OF MANUAL

This manual provides general service and preventive maintenance information for the ANRITSU 373XXA family of Vector Network Analyzer (VNA) systems. It contains procedures for:

- Testing the instrument for proper operation.
- Verifying measurement accuracy and traceability to National Institute of Standards and Technology (NIST).
- Troubleshooting a failed instrument to the exchange subassembly level or the subsystem requiring adjustment.
- Adjusting instrument internal sub-systems.
- Locating and replacing failed parts.

Throughout this manual, the terms "373XXA" and "373XXA VNA" will be used interchangeably to refer to all Series 37300A Network Analyzer system models, unless otherwise noted.

## 1-2 INTRODUCTION

This chapter of the manual provides a general description of 373XXA VNA systems, system serial numbers, frequency ranges, and related manuals. Also included is information about the level of maintenance covered in this manual, service strategy, available service facilities, and static-sensitive component handling precautions. A list of recommended test equipment is also provided.

## 1-3 IDENTIFICATION NUMBER

All ANRITSU instruments are assigned a six-digit ID number, such as "401001". This number appears on a decal affixed to the rear panel. Please use this identification number during any correspondence with ANRITSU Customer Service about this instrument.

## 1-4 ONLINE MANUAL

This manual is available on CD ROM as an Adobe Acrobat™ (*.pdf) file. The file can be viewed using Acrobat Reader™, a free program that is also available on the CD ROM. This file is "linked" such that the viewer can choose a topic to view from the displayed "bookmark" list and "jump" to the manual page on which the topic resides. The text can also be word-searched. Contact ANRITSU Customer Service for price and availability.

## 1-5 SYSTEM DESCRIPTION

*373XXA Model Frequencies*

| Model | Freq Range |
|---|---|
| 37317A | 22.5 MHz to 8.6 GHz |
| 37325A | 40.0 MHz to 13.5 GHz |
| 37347A | 40.0 MHz to 20.0 GHz |
| 37369A | 40.0 MHz to 40.0 GHz |
| 37397A | 40.0 MHz to 65.0 GHz |

The 373XXA Analyzers are microprocessor controlled Vector Network Analyzers. Each is a single-instrument system that contains a built-in signal source, a test set, and an analyzer subsystem. A typical model (37369A) is shown in Figure 1-1. These analyzers are produced in five models that cover a range of from 22.5 MHz to 65 GHz. The table at left lists the frequencies for each model.

## 1-6 RELATED MANUALS

The 373XXA Vector Network Analyzer Operation Manual (10410-00183) describes the front panel operation for all 373XXA models. It also contains general information, specifications, and Performance Verification procedures for all models.

The 37XXX Series Vector Network Analyzer Programming Manual (10410-00200) describes all 373XXA GPIB commands and provides programming information for operation of the 373XXA remotely via the IEEE-488 General Purpose Interface Bus. Included at the rear of this manual is the 37XXX Series Vector Network Analyzer GPIB Quick Reference Guide (10410-00201).

Model 360X/373XXA VNA Performance Verification Software Users Guide, P/N: 10410-00208 (located in Appendix E at the rear of this manual). This Software Users Guide explains in detail the procedures to be used for the installation and operation of the 373XXA VNA Verification Software on your computer/controller.

## 1-7 STANDARD OPTIONS

The standard 373XXA VNA options and their respective Upgrade Kit part numbers are:

| Option* | Description | Upgrade Kit |
|---|---|---|
| Opt 1 | Rack Mount with slides | ND39486 |
| Opt 1A | Rack Mount | ND40916 |
| Opt 2A | Time Domain (Microwave Units) | ND39477 |
| Opt 2B | Time Domain (RF Units) | ND40914 |
| Opt 10A | High Stability Ovenized Time Base | ND45045 |

* All options listed can be installed at ANRITSU Service Centers

## 1-8 SERVICE STRATEGY

This paragraph provides an overview of the 373XXA VNA service strategy and available service facilities. It also provides references to the information in various locations in this manual needed to accomplish the service functions required for the 373XXA VNA.

Appendices - Refer to the Appendices at the rear of this manual for detailed descriptions of the following:

- Diagnostics Menus and GPIB Commands.
- Error Messages.
- System Block Diagrams.
- Parts Locator Diagrams.

***Functional Assembly Level Troubleshooting***

The 373XXA modular design, extensive built-in diagnostics, and automated service tools are designed to support fast exchange of functional assembly level repairs.

Failed assemblies are not field repairable. Once an assembly is found to be faulty, it should be returned to an authorized ANRITSU Service Center for exchange. Refer to the description of the Exchange Assembly Program in Chapter 2, Replaceable Parts.

The procedures for troubleshooting a failed 373XXA VNA are described in this manual in Chapter 5, Troubleshooting.

***Internal Hardware Adjustments and Calibrations***

There are five automated internal hardware field calibrations. Two of them are used to characterize the 373XXA frequency and power generation sub-systems. These calibrations insure fast, consistent phase lock of system frequencies and proper compensation, leveling, and flatness of system power at the front panel test ports.

To conduct these calibrations, you need only connect the appropriate test equipment (counter or power meter) to the 373XXA and initiate the calibration. The 373XXA will control itself and the externally connected test equipment to perform measurements and store calibration constants in its internal battery backed RAM (BBRAM).

The procedures for adjusting the 373XXA VNA are described in this manual in Chapter 6, Adjustments.

***Internal Service Log***

The 373XXA continuously monitors itself for proper operation. Should a failure occur, it notifies the user via a failure message on the display screen. (In remote-only operation, it also sets the GPIB Status Byte, if enabled.) It also writes the error message along with some data pertinent to the failure to an internal service log stored in battery backed memory.

The service log can be checked at any time to view (without erasing) all error messages that were written into it. It is capable of storing

more than 30 pages of service messages and data. The 373XXA will automatically remove the oldest errors first to make room for new errors, if necessary. To check the contents of the service log, use the procedure described in Chapter 3, Operational Tests.

***NOTE***

A printed or disk file copy of the Service Log (with the failure in question) must be made available to ANRITSU when exchanging a failed assembly, or when requesting service support. Refer to Chapter 2, Replaceable Parts, for further information.

***System Test/Certification***

Quick operational checkout of the system may be accomplished by the system user or for incoming inspection purposes using the "Operational Checkout" chapter in the 373XXA Operations Manual. Those procedures are useful in quickly verifying that the instrument's primary measurement functions are operational and stable.

Full operational testing of the system is detailed in Chapter 3, Operational Tests. These tests should be performed annually, or more often depending on system use.

Verification of the system's measurement accuracy and other key performance parameters may be done using the procedures in Chapter 4, Performance Verification. This should be performed annually, or more often depending on system use.

***Preventive Service***

The 373XXA A9 Processor PCB contains a battery backed memory/real time clock chip (BBRAM) and a static memory (SRAM) backup battery. These have a finite life span and should be replaced periodically per the procedures in Chapter 8, Removal and Replacement Procedures.

The BBRAM chip has a rated life span of 4 years. The SRAM backup battery has a worst case elapsed time for SRAM battery protection of 200 days. The SRAM battery life span will vary according to how the system is used; that is, how often the system is powered off for extended periods of time.

***Servicing Specially Modified Instruments***

Instruments with customer requested special modifications performed by ANRITSU will have an identifying Specials Modification number printed on the rear panel. This number will be preceded with the letters SM, i.e., SM1234 is special modification number 1234.

Special instruments may have service requirements different from those specified in this manual. Contact your local Service Center if you need more information when servicing such instruments.

## 1-9 SERVICE SUPPORT

The following paragraphs briefly describe the various service support services and aids available to you to help you maintain your 373XXA.

***Technical Support***

Technical service support is available by contacting any ANRITSU Worldwide Service Center (refer to paragraph 1-11). Or, service support may be obtained directly from the factory by contacting:

ANRITSU Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

If servicing or repairing your own system and you need technical support, you will need to FAX or mail a printout of the items listed below to the ANRITSU Customer Support Engineer:

- Measurement data in question
- "Operational Tests" results
- System state (from UTILITY menu)
- Service Log (from DIAGNOSTICS menu)

***Field Service Kits***

The field service kit listed below is available through your local ANRITSU Sales or Service Center:

**ND37200A-2, Field Service Kit**

This kit provides for automated field test and performance verification of the 373XXA. It is packaged in a hardened rolling case that also has space for two, user supplied, verification and calibration kits and other accessories.

The ND37200A-2, Field Service Kit is comprised of all major subassemblies of all models 40 Ghz and below high-end frequency.

**ND53269, Field Service Kit**

This kit provides for automated field test and performance verification of the 373XXA 50 and 65 GHz models (37397A). It supplements kit ND37200A-2.

***Service Software***

The service software listed below is contained on the diskette located at the rear of this manual:

**ANRITSU 37XXX Test Software (2300-178).**

This software contains a series of automated tests designed to insure the 373XXA signal paths are functioning properly and capable of supporting stable calibrations and measurements. See Operational Tests Chapter for details.

**ANRITSU 37XXX Performance Verification Software (2300-237).**

This software is used to verify the 373XXA published measurement accuracy and traceability to the U.S. National Institute of Standards and Technology (NIST). See Chapter 4, Performance Verification, for details.

***Verification Kits***

The ANRITSU Verification Kits listed below are used in conjunction with the 37XXX Performance Verification Software (above). See Chapter 4, Performance Verification, for further information.

**N Verification Kit (Model 3663)**

Contains precision N Connector components with characteristics that are traceable to the NIST.
Use for Models 37317A and below with Option 7N and 7 NF.

**3.5 mm Verification Kit (Model 3666)**

Contains precision 3.5 mm Connector components with characteristics that are traceable to the NIST.
Use for Models 37347A and below with Option 7A.

**GPC-7 Verification Kit (Model 3667)**

Contains precision GPC-7 Connector components with characteristics that are traceable to the NIST.
Use for Models 37317A and below with Option 7A.

**K Verification Kit (Model 3668)**

Contains precision K Connector components that are traceable to the NIST.

**V Verification Kit (Model 3669B)**

Contains precision V Connector components that are traceable to the NIST.

***Test Fixtures/ Aids***

The test fixtures and test aids listed below are available through your local ANRITSU Sales or Service Center:

**Rear Panel Printer Port Test Fixture (B39553).**

This test fixture is used to check out digital printer interface circuits on the rear panel assembly.

**GPIB Cable (2100-2).**

This cable is used to check out digital GPIB interface circuits on the rear panel assembly.

***Failed Assembly Exchange Program***

The exchange program allows a customer to quickly exchange a failed subassembly for a factory refurbished, fully system-tested and unit that is under warranty. This results in significant time and price savings as compared with ordering a new assembly.

Refer to Chapter 2, Replaceable Parts, for a complete list of exchangeable assemblies for all Series 373XXA models.

***NOTE***

When sending a failed assembly to the factory for exchange, a copy of the Service Log **must always** accompany the failed assembly. Refer to Chapter 2, Replaceable Parts, for further information.

## 1-10 PERFORMANCE SPECIFICATIONS

The performance specifications for all Series 373XXA models are contained in the Technical Data Sheets that are located in Appendix D, Performance Specifications.

## 1-11 SERVICE CENTERS

ANRITSU Company offers a full range of repair and calibration services at fully staffed and equipped service centers throughout the world. Table 2-1, located on page 2-4, lists all ANRITSU services centers.

## 1-12 STATIC SENSITIVE COMPONENT HANDLING PROCEDURES

The 373XXA contains components that can be damaged by static electricity. Figure 1-2 illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

## 1-13 RECOMMENDED TEST EQUIPMENT

Table 1-1 lists the recommended test equipment to be used for all maintenance activities for all Series 373XXA models. Note the "Use" codes listed in the right hand column of the table. These codes list the applicable maintenance activities for the equipment listed.

**Table 1-1.** *Recommended Test Equipment (1 of 2)*

| INSTRUMENT | CRITICAL SPECIFICATION | RECOMMENDED MANUFACTURER/MODEL | USE** |
|---|---|---|---|
| Computer/Controller | PC with Windows 95 or later and National Instruments GPIB hardware and software. | Any | O, P |
| Test Software | | ANRITSU 2300-178 | O |
| Floppy Disk | Formatted, IBM PC format | DS/HD 1.44 Mbyte | A |
| GPIB Cable | | ANRITSU 2100-2, or equivalent | O, P, A |
| RF/Microwave Cable | DC – 40 GHz, K type connectors (male or female), Length, 3 ft. | Any | P, A |
| BNC Cable | Length, 4 ft., 2 each | Any | O |
| Printer Port Test Fixture | | ANRITSU B39553 | O |
| Thru Line | For models 37317A and below<br>For models 37325A and above: | ANRITSU 3670A50-2, 3671A50-2<br>ANRITSU 3670K50-2, 3671K50-2 | O, P |
| Calibration Kit | For models 37317A and below, with Opt 7A:<br>For models 37317A and below, with Opt 7N or 7NF:<br>For models 37325A and above:<br>For models 37325A and below, with Opt 7S:<br>For model 37397A | ANRITSU 3651-1*<br>ANRITSU 3653<br>ANRITSU 3652-1*<br>ANRITSU 3650-1*<br>ANRITSU 3654B | O, P |
| Performance Verification Software | | ANRITSU 2300-237 | P |
| Connector Verification Kit | For models 37217B and below w/Opt 7A:<br>For models 37217B and below, with Opt 7N or 7NF:<br>For models 37225B and above:<br>For models 37247B and below, with Opt 7S:<br>For model 37397A | ANRITSU 3667<br>ANRITSU 3663<br>ANRITSU 3668<br>ANRITSU 3666<br>ANRITSU 3669B | P |

* Calibration Kit sliding load (Option {-1}), required for Performance Verification only.

** USE CODES:
- A Adjustment / Internal Hardware Calibration
- O Operational Testing
- P Performance Verification
- T Troubleshooting

**Table 1-1.** *Recommended Test Equipment (2 of 2)*

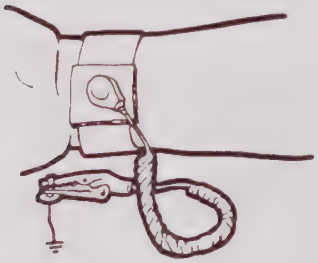
| INSTRUMENT | CRITICAL SPECIFICATION | RECOMMENDED MANUFACTURER/MODEL | USE** |
|---|---|---|---|
| Assurance Air Line | For models 37317A and below w/Opt 7A:<br>For models 37317A and below w/Opt 7N:<br>For models 37317A and below w/Opt 7NF:<br>For models 37317A and above:<br>For models 37317A and below w/Opt 7S: | ANRITSU 18A50<br>ANRITSU 18NF50<br>ANRITSU 18N50<br>ANRITSU T1519<br>ANRITSU T1147-2 | P |
| Offset Termination | For models 37317A and below w/Opt 7A, 7N, 7NF:<br>All other models | ANRITSU 29A50-20<br>ANRITSU 29KF50-15 | P |
| Frequency Counter | *Frequency:* 0.1 to 26.5 GHz<br>*Input Impedance*: 50Ω | EIP Microwave, Inc., Model 578B | P, A |
| Digital Multimeter | *Resolution:* 4½ digits<br>*DC Accuracy:* 0.1 %<br>*AC Accuracy:* 0.1 % | Any | T |
| Oscilloscope | *Bandwidth:* DC to 100 MHz<br>*Sensitivity:* 2 mV<br>*Horiz. Sensitivity:* 50 ns/division | Tektronix, Inc.<br>Model 2445 | T |
| Power Meter 1, with:<br><br>Power Sensor 1<br>***or:***<br>Power Meter 2, with:<br>Power Sensor 2 | *Power Range:* –30 to +20 dBm<br>(1 mW to 100 mW)<br>*Other:* GPIB controllable<br><br>*Frequency Range:* 0.05 to 50 GHz<br>*Power Range:* –70 to +47 dBm<br>(100 pW to 50 W)<br>*Other:* GPIB controllable<br>*Frequency Range:* 0.01 to 40 GHz | HP 437B with Option 22 (GPIB)<br><br>HP 8487A<br><br>Gigatronics 8541 or 8542<br>Gigatronics 80304A | P, A<br><br>P, A |
| Power Meter and Power Sensor | Frequency Range: to 65 GHz | Anritsu Model ML24xxA Power Meter and MA2474A (40 GHz and below) and Model SC6230 (to 65 GHz) Power Sensors | P, A |
| Gauging Set | GPC-7 Gauging Set<br>K Connector Gauging Set | ANRITSU 01-161<br>ANRITSU 01-162 | O, T |

** USE CODES:
- A Adjustment / Internal Hardware Calibration
- O Operational Testing
- P Performance Verification
- T Troubleshooting

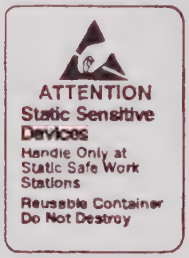
1. Do not touch exposed contacts on any static sensitive component.

2. Do not slide static sensitive component across any surface.

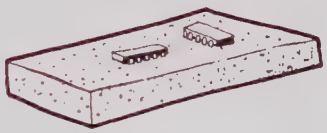
3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.



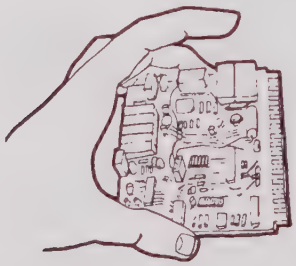
4. Wear a static-discharge wristband when working with static sensitive components.



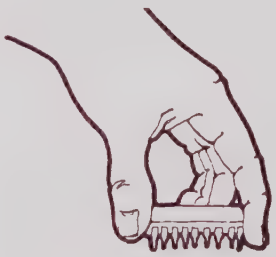

5. Label all static sensitive devices.



6. Keep component leads shorted together whenever possible.



7. Handle PCBs only by their edges. Do not handle by the edge connectors.



8. Lift & handle solid state devices by their bodies – never by their leads.

9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

**Figure 1-2.** *Static Sensitive Component Handling Procedures*

# *Chapter 2*
# *Replaceable Parts*

## *Table of Contents*


| | | |
|---|---|---|
| 2-1 | INTRODUCTION | 2-3 |
| 2-2 | EXCHANGE ASSEMBLY PROGRAM | 2-3 |
| 2-3 | REPLACEABLE SUBASSEMBLIES AND PARTS | 2-3 |
| 2-4 | PARTS ORDERING INFORMATION | 2-4 |

# Chapter 2
# Replaceable Parts

## 2-1 INTRODUCTION

This chapter provides replaceable parts information for all 373XXA models. The major replaceable 373XXA assemblies and parts are listed in Tables 2-2 through 2-8. The locations of these assemblies/parts are shown in Figures 2-1 through 2-4.

## 2-2 EXCHANGE ASSEMBLY PROGRAM

ANRITSU maintains a module exchange program for selected subassemblies. If a malfunction occurs in one of these subassemblies, the defective item can be exchanged. Upon receiving your request, ANRITSU will ship the exchange subassembly to you, typically within 24 hours. You then have 45 days in which to return the defective item. All exchange subassemblies or RF assemblies are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

***NOTE***

When sending a failed assembly to the factory for exchange, a copy of the Service Log **must always** accompany the failed assembly. This copy may be a printout, or a saved disk copy. Due to the importance of the service log information to the ANRITSU factory Service Engineers, the exchange prices are only valid if the service log data is included with the failed assembly.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local sales representative or call ANRITSU Customer Service direct (refer to paragraph 2-4.

## 2-3 REPLACEABLE SUBASSEMBLIES AND PARTS

Tables 2-2 through 2-5, (starting page 2-5) list the major replaceable subassemblies and parts for the 373XXA. These assemblies/parts are presently covered by the ANRITSU exchange assembly program. Table 2-6 (page 2-6) lists disposable parts for the 373XXA, and Table 2-7 and 2-8 lists factory-repairable parts for the 373XXA. (The parts listed in Tables 2-6 through 2-8 are not presently on the exchange assembly program.)

***NOTE***

The 373XXA A17 Motherboard PCB Assembly is not a field-replaceable item.

## 2-4 PARTS ORDERING INFORMATION

All parts listed in Tables 2-2 through 2- 8 may be ordered from your local ANRITSU service center (Table 2-1). Or, they may be ordered directly from the factory at the following address:

ANRITSU Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

*Table 2-1. ANRITSU Service Centers*

**UNITED STATES**

ANRITSU COMPANY
490 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 778-2000
FAX: (408) 778-0239

ANRITSU ANRITSU COMPANY
685 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 776-8300
FAX: (408) 776-1744

ANRITSU ANRITSU COMPANY
10 Kingsbridge Road
Fairfield, NJ 07004
Telephone: (201) 227-8999
FAX: (201) 575-0092

**AUSTRALIA**

ANRITSU PTY. LTD.
Level 2, 410 Church Street
North Parramatta
NSW 2151 Australia
Telephone: 026-30-81-66
Fax: 026-83-68-84

**BRAZIL**

ANRITSU ANRITSU ELECTRONICA LTDA.
Praia de Botafogo, 440-SL 2401-Botafogo
2225-Rio de Janeiro-RJ-Brasil
Telephone: 021-28-69-141
Fax: 021-53-71-456

**CANADA**

ANRITSU ANRITSU INSTRUMENTS LTD.
215 Stafford Road, Unit 102
Nepean, Ontario K2H 9C1
Telephone: (613) 828-4090
FAX: (613) 828-5400

**CHINA**

ANRITSU BEIJING SERVICE CENTER
416W Beijing Fortune Building
5 Dong San Huan Bei Lu
Chao Yang Qu, Beijing 100004, China
Telephone: 86-1-50-17-559
FAX: 86-1-50-17-558

**FRANCE**

ANRITSU ANRITSU S.A
9 Avenue du Quebec
Zone de Courtaboeuf
91951 Les Ulis Cedex
Telephone: 016-44-66-546
FAX: 016-44-61-065

**GERMANY**

ANRITSU ANRITSU GmbH
Rudolf Diesel Strabe 17
8031 Gilching
Telephone: 08-10-58-055
FAX: 08-10-51-700

**INDIA**

MEERA AGENCIES (P) LTD.
A-23 Hauz Khas
New Delhi 110 016
Telephone: 011-685-3959
FAX: 011-686-6720

**ISRAEL**

TECH-CENT, LTD
Haarad St. No. 7, Ramat Haahayal
Tel-Aviv 69701
Telephone: (03) 64-78-563
FAX: (03) 64-78-334

**ITALY**

ANRITSU ANRITSU Sp.A
Roma Office
Via E. Vittorini, 129
00144 Roma EUR
Telephone: (06) 50-22-666
FAX: (06) 50-22-4252

**JAPAN**

ANRITSU CORPORATION
1800 Onna Atsugi-shi
Kanagawa-Prf. 243 Japan
Telephone: 0462-23-1111
FAX: 0462-25-8379

**KOREA**

ANRITSU CORPORATION
#2103 Korea World Trade Center
159-1 Samsung-Dong
Kangnam-ku, Seoul
Telephone: (02) 551-2250
FAX: (02) 551-4941

**SINGAPORE**

ANRITSU ANRITSU (SINGAPORE) PTE LTD
3 Shenton Way #24-03
Shenton House
Singapore 0106
Telephone: 011-65-2265206
FAX: 011-65-2265207

**SWEDEN**

ANRITSU ANRITSU AB
Box 247
S-127 25 Skarholmen
Telephone: (08) 74-05-840
FAX: (08) 71-09-960

**TAIWAN**

ANRITSU CO., LTD.
8F, No. 96, Section 3
Chien Kuo N. Road
Taipei, Taiwan, R.O.C.
Telephone: (02) 515-6050
FAX: (02) 509-5519

**UNITED KINGDOM**

ANRITSU ANRITSU LTD.
200 Capability Green
Luton, Bedfordshire
LU1 3LU, England
Telephone: 05-82-41-88-53
FAX: 05-82-31-303

*Table 2-2. Printed Circuit Board Assemblies*

| Reference Designator | 373XXA Option | Assembly / Part | Part Number |
|---|---|---|---|
| A1 | | LO1 | D46866-3 |
| A1 | | LO1 | D86866-4* |
| A2 | | LO2 | D50725-3 |
| A3 | | Test A IF | D38503-4 |
| A4 | | Reference IF | D41794-3 |
| A4 | | Reference IF | D41794-4* |
| A5 | | A/D | D38505-3 |
| A6 | | Test B IF | D38503-5 |
| A7 | | LO3 | D38507-3 |
| A7 | Opt 10 | LO3 | D38507-4 |
| A8 | | Source Lock/ Separation Control | D47488-3 |
| A8 | | Source Lock/ Separation Control | D49334-3* |
| A9 | | Main Processor | B38509 |
| A13 | | I/O #1 | D38513-3 |
| A14 | | I/O #2 | D38514-3 |
| A15 | | Graphics Processor | D44281-3 |
| A16 | | Hard Disk (w/ PCB) | D41041-3 |
| A18 | | Rear Panel PCB | D44255-3 |
| A19** | | Front Panel Switch PCB | See Table 2-5 |
| A20** | | Front Panel Control PCB | |
| A21A1 | | Source YIG/Bias Control (p/o Signal Source Module) | D48516-3 |
| A21A1 | | Source YIG/Bias Control (p/o Signal Source Module) | D48512-3* |
| A21A2 | | Source Control (p/o Signal Source Module) | D41841-3 |
| A21A2 | | Source Control (p/o Signal Source Module) | D48513-3* |
| A24 | | VME Bus Terminator | D38524-3 |

* Required for 37397A
** Part of the Front Panel Assembly (refer to Table 2-5).

*Table 2-3. Test Set Assembly RF / Microwave Components, 37317A, 37325A, 37347A, 37369A*

| Assembly / Part | 373XXA Model / Option | Part Number |
|---|---|---|
| Transfer Switch | All | D28580-1<br>46535* |
| Step Attenuator, 70 dB | All | 4612K |
| Low Frequency Bridge w/ Bias Tee | 37311A, 37317A | D28985 |
| Coupler w/ Bias Tee | 37325A and higher | D28967 |
| 40 GHz Quad Buffer Amp/Power Amplifier | 37369A only | ND47533 |
| Switched Doubler Module (SDM) | 37369A only | D28685 |
| Port 2 Step Attenuator | All | 4612K |
| 6 dB Pad | 37369A only | 43KC-10 |
| 20 dB Pad | 37347A and below | 43KC-20 |
| 20 GHz Quad Buffer Amp/Power Amplifier | All except 37369A | ND47532 |

* Used on serial numbers 975004, 975101, 975103, 980102, 980104, 980201, 980302, 980402, 980403, 980405, 980406, 980407, 980602, 980603, 980701, and above.

*Table 2-4. Test Set Assembly RF / Microwave Components, 37397A*

| Assembly / Part | Part Number |
|---|---|
| Pinswitch | 29855 |
| Switched Doubler Module (SDM) | 47520 |
| Quadrupler (SQM) | 48998 |
| 37GHz High Pass Filter | 49247 |
| Mux Coupler (Port 1) | 49470 |
| Mux Coupler (Port 2) | 49480 |
| Shaped Pad | 52956 |
| Bias Tee | 53409 |
| 16.8 GHz Lowpass Filter | B28912 |
| Access Loops (Front and Rear Panel) | B35569-195 |
| Transfer Switch | D27030 |
| 3 dB Fixed Attenuator | ND26178 |
| Step Attenuator | ND52564 |
| Coupler | ND52929 |
| Quad Buffer Amplifier/Power Amplifier | ND53249 |

*Table 2-5. Miscellaneous /Integrated Assemblies*

| Assembly / Part | 373XXA Model / Option | Part Number |
|---|---|---|
| 10 MHz Ovenized Oscillator | Opt 10 only | ND39476 |
| Power Supply Module | All | 40-116 |
| VGA Monitor | All | 2000-322 |
| Floppy Disk Assy | All | C38550 |
| Front Panel Assy (w/ Front Panel, A19 and A20 PCB's, and all Model ID Overlays) | All | ND42700 |
| Fan Assembly, Rear Panel | All | B38533 |
| Front Panel Assy (incudes front panel, A19 and A20 PCBs, and all model ID overlays) | LCD Equipped | ND44606 |
| Power Supply | LCD Equipped | 40-114 |
| Liquid Crystal Display (LCD) | LCD Equipped | 15-88 |
| Liquid Crystal Display (LCD) | LCD Equipped SN:972701 and above | 15-92 |
| Liquid Crystal Display (LCD) | LCD Equipped SN:994600 and above | 15-100 |

*Table 2-6. Consummsable Parts*

| Assembly / Part | 373XXA Model / Option | Part Number |
|---|---|---|
| System Software | All | 2300-212 |
| Front Panel Encoder Knob | All | 2000-577 |
| Front Panel Amber Lens | All | 790-412 |
| Fuse, 8A, Fast Blow 3AG Cartridge type (F1 Line fuse for power supply assembly) | All | 631-72 |
| Battery Backed RAM | All | 54-1350 |
| Back-Up Battery | All | 633-20 |
| LCD Back Light Driver PCB | LCD Equipped | 2000-770 |
| LCD Back Light Lamp | LCD Equipped | 632-55 |

*Table 2-7. Signal Source Module RF / Microwave Components*

| Assembly / Part | 373XXA Model / Option | Part Number |
|---|---|---|
| YIG Oscillator (2 - 20 GHz) | All | C21620-1 |
| Down Converter | All | D27532 |
| Switched Filter | 37317A and below | D45243 |
| Switched Filter | 37325A and above | D45244 |

*Table 2-8. Factory Repairable Non-Exchange Parts*

| Assembly / Part | 373XXA Model / Option | Part Number |
|---|---|---|
| Test Port Connector, K-Male | All | 34UK50 |
| Test Port Connector, GPC-7 | Opt 7A only | 34UA50 |
| Test Port Connector, 3.5 mm | Opt 7S only | 34US50 |
| Test Port Connector, type N | Opt 7N only | 34UN50 |
| Test Port Connector, type NF | Opt 7NF only | 34UNF50 |
| Test Port Connector, V | 37397A | 34YV50 |

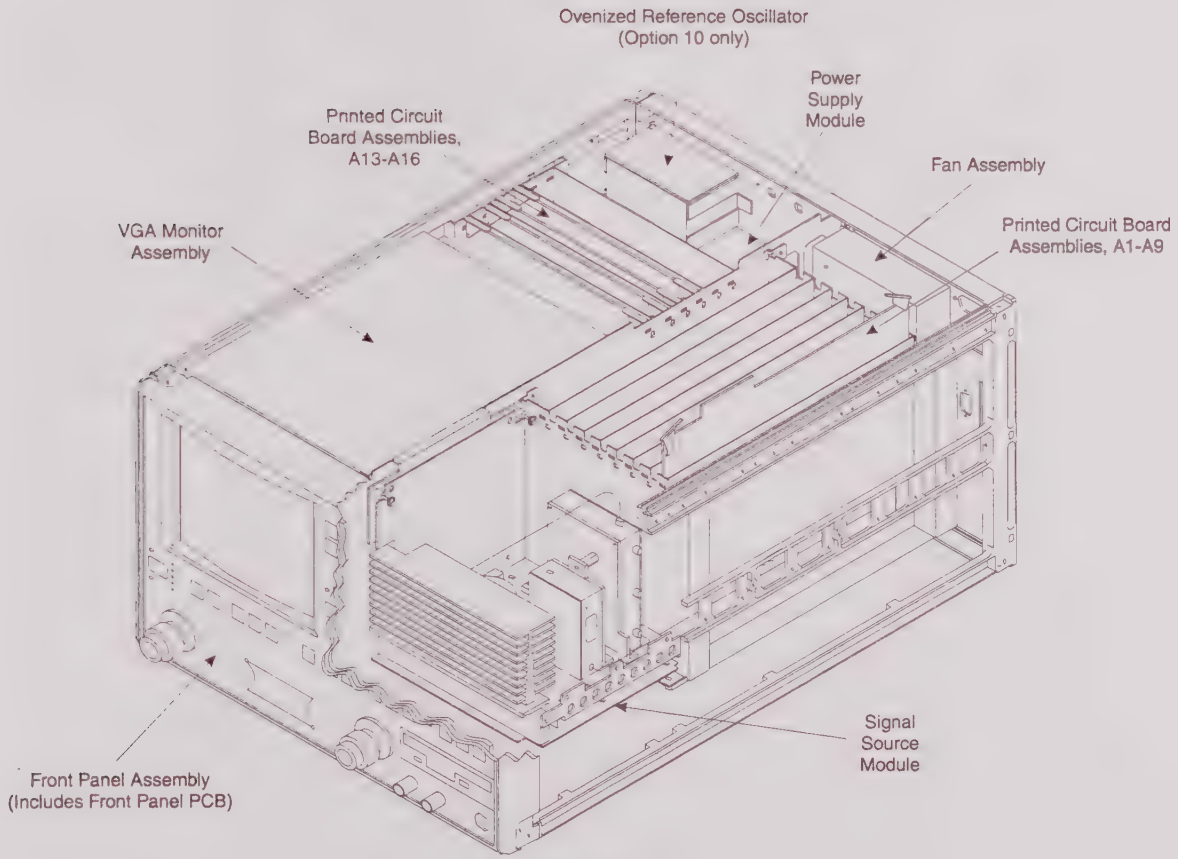



**Figure 2-1.** *Major Assemblies Location Diagram (Top ¾ View)*

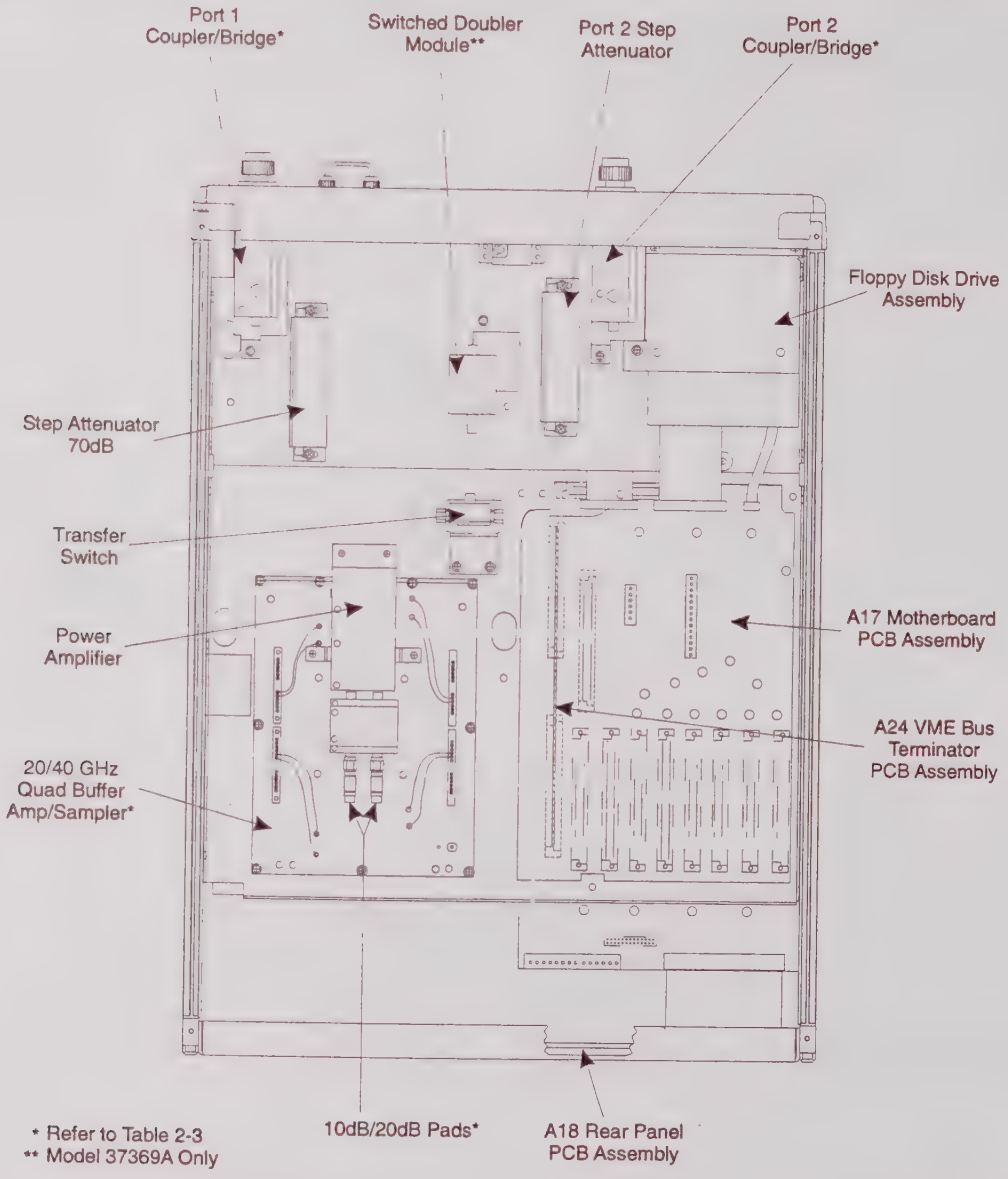



**Figure 2-2.** *Major Assemblies Location Diagram (Bottom View) (Not 37397A)*

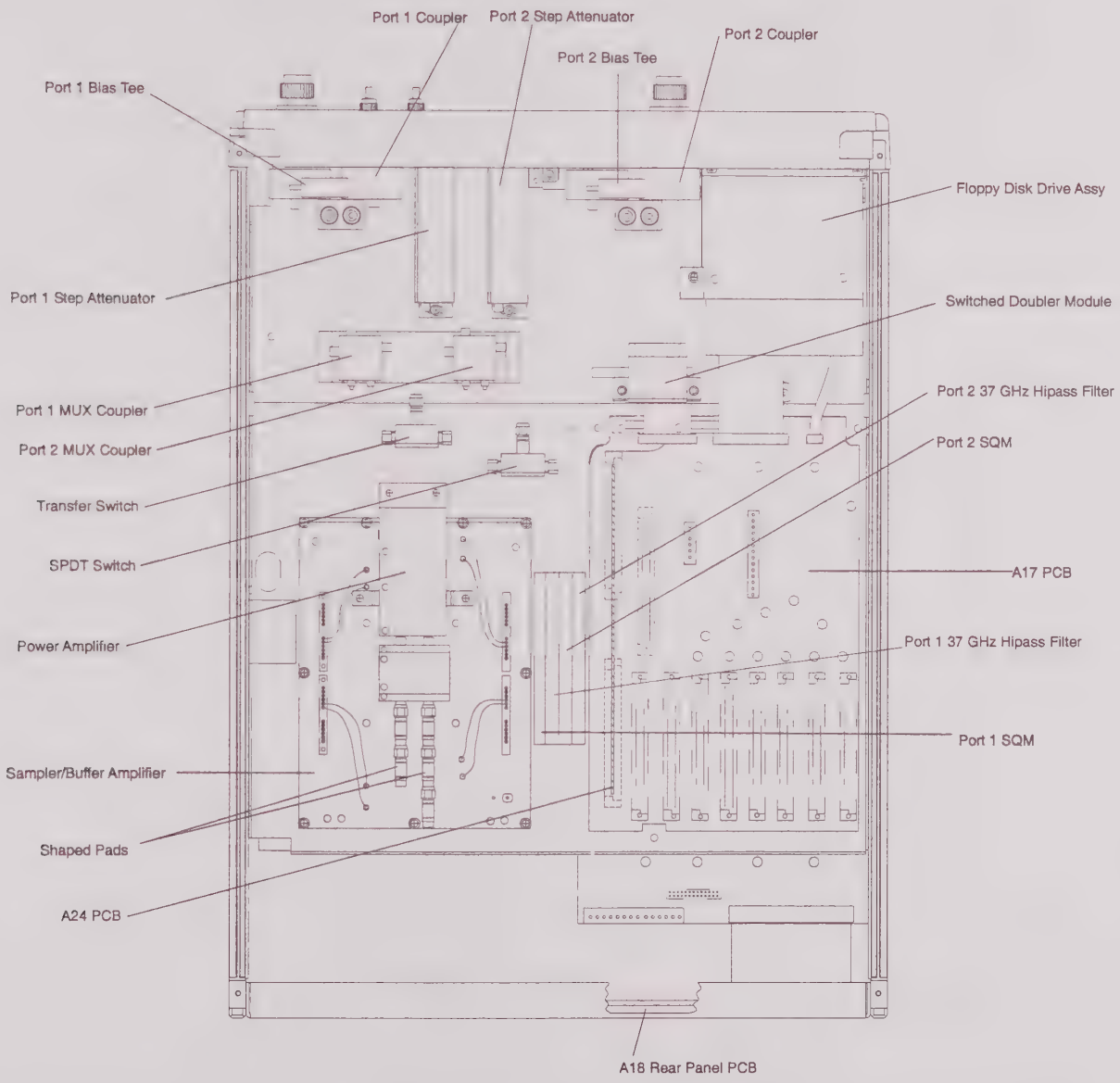



**Figure 2-3.** *Major Assemblies Location Diagram (Bottom View) (37397A)*

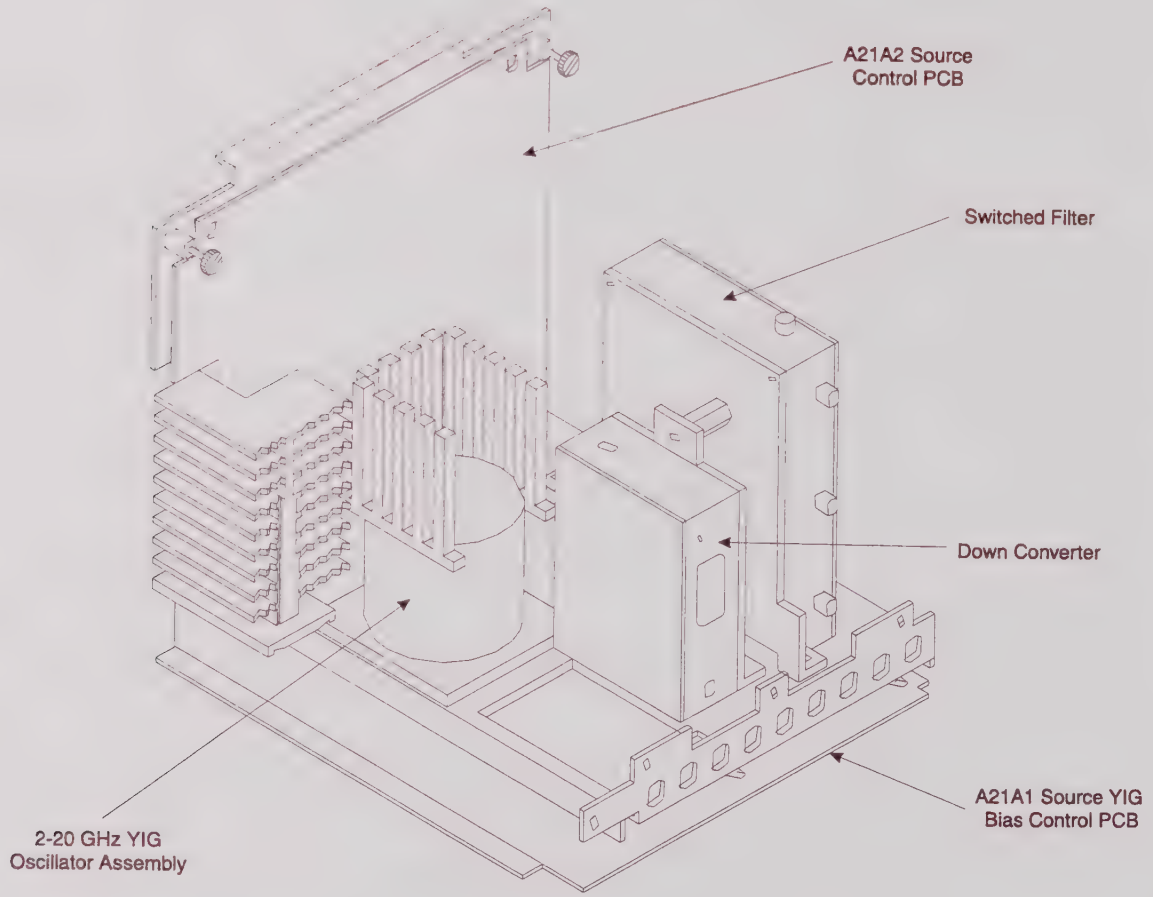



**Figure 2-4.** *Signal Source Parts Location Diagram*

# *Chapter 3*
# *Operational Tests*

## *Table of Contents*


| | | |
|---|---|---|
| 3-1 | INTRODUCTION | 3-3 |
| 3-2 | CHECKING THE SERVICE LOG | 3-4 |
| 3-3 | SELF TEST | 3-5 |
| 3-4 | PERIPHERALS AND INTERFACES | 3-6 |
| | LCD Test | 3-6 |
| | Front Panel Test | 3-7 |
| | External Keyboard Interface Test | 3-7 |
| | Printer Interface Test | 3-7 |
| | GPIB Interface Test | 3-9 |
| 3-5 | SIGNAL PATH | 3-10 |

# Chapter 3
# Operational Tests

## 3-1 INTRODUCTION

The tests in this section provide a means of fully testing the 373XXA VNA system for proper operation and signal stability. These tests are intended to be used as a periodic check of the operational functionality of the 373XXA.

The tests should be performed in their entirety at least once annually. Although there is no requirement to do so, the tests should generally be run in the sequence presented.

***NOTE***

The procedures presented in Chapter 4, Performance Verification, provide the means to test the *accuracy* of the tests performed by the 373XXA.

Please ensure you have read and fully understand the servicing concepts for the 373XXA presented in Chapter 1 prior to continuing with this chapter.

Operational Tests for the 373XXA consist of the following:

- Checking the Service Log
- Self Test
- Peripherals and Interface Testing
- Signal Path Tests (includes Checking the Service Log and Self Test.)

These tests are described in paragraphs 3-2 through 3-5, which start on the next page.

## 3-2 CHECKING THE SERVICE LOG

Checking the service log consists of viewing the entries written into the log.

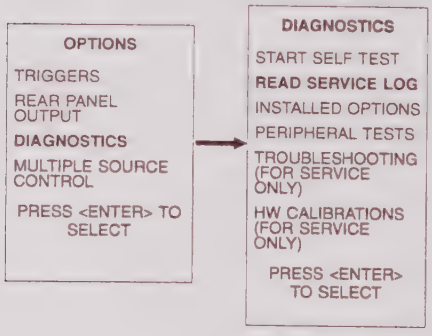
***CAUTION***

The service log contains historical information about instrument condition and any failures that may have occurred. It should be cleared only by a qualified service engineer. Such clearing shuld be accomplished only upon determining that the errors need not be saved to disk, or printed out for service purposes.

***Procedure:***

***Step 1.*** Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

***Step 2.*** Select **DIAGNOSTICS** from menu (left); then select **READ SERVICE LOG** from the DIAGNOSTICS menu.




The 373XXA will now display the contents of the service log. The display consists of a header and an error listing. The header contains a variety of system service information. The error listing contains error messages for failures that may have occurred during operation.

***NOTE***

- Errors 7201–7209, GPIB remote operation programming errors, report that one or more external GPIB programming errors has been detected. These messages do not indicate a 373XXA system fault.
- Informational messages 0000–0099 report the pass/fail status of a peripheral access. These messages do not indicate a 373XXA system fault.

Any other error messages in the service log may indicate an instrument problem and should be investigated. Refer to the Chapter 5, Troubleshooting, for further information.

***CAUTION***

The **CLEAR SERVICE LOG** menu selection will immediately and permanently clear all the error message entries from the service log. (However, it will not clear the header information.) See Caution message at top of page.

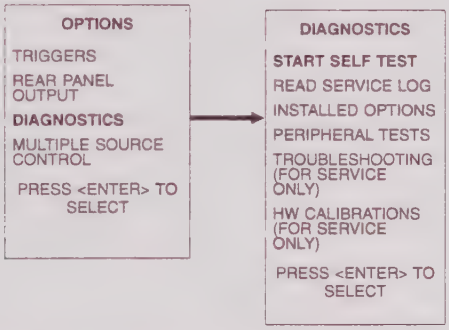
## 3-3 SELF TEST

The self test performs a series of tests that verify that various internal 373XXA circuits are functional and operating properly.

***To start the self test:***

***Step 1.*** Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

***Step 2.*** Select **DIAGNOSTICS** from menu; then select **START SELF TEST** (below).




***Step 3.*** Wait for test sequence to complete. (Once invoked, this test requires no user interaction or external equipment.)

Upon completion, the net pass/fail result of the self test is shown on the CRT display. If the 373XXA is in remote-only operation, the results are reported via the GPIB output buffer. If the self test fails, detailed error messages will be written into the service log.

***If self test fails:***

- ❑ Check the service log to view failure messages.
- ❑ Proceed to Chapter 5, Troubleshooting.

## 3-4 PERIPHERALS AND INTERFACES

These tests are used to verify the operation of the liquid-crystal display (LCD), front panel keys, and peripheral devices that are used with the 373XXA. They consist of the following:

- LCD Test
- Front Panel Test
- External Keyboard Interface Test
- Printer Interface Test
- GPIB Interface Test

### *LCD Test*

This test verifies that the 373XXA LCD is functioning correctly.

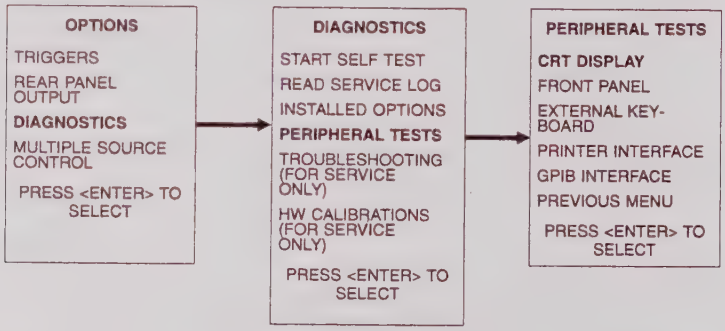
***NOTE***

The External VGA Out Connector can also be tested when using this procedure if an external VGA monitor is connected.

***Procedure:***

***Step 1.*** Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

***Step 2.*** Select **DIAGNOSTICS** from menu; then in sequence select: **PERIPHERAL TESTS**, and then **CRT DISPLAY**. See diagram below.




***Step 3.*** Follow instructions on the CRT screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

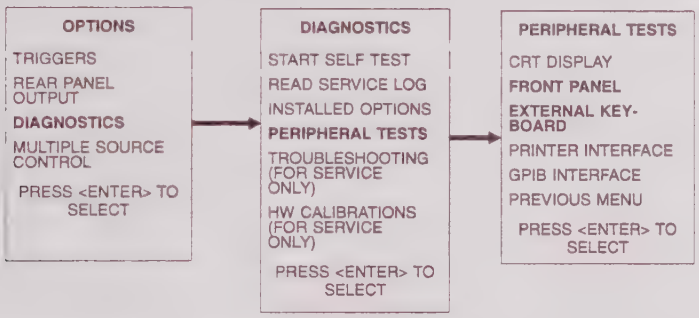
***Front Panel Test***

This test verifies that the control keys in each of the 373XXA key groups are functioning correctly.

***Procedure:***

***Step 1.*** Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

***Step 2.*** Select **DIAGNOSTICS** from menu; then in sequence select: **PERIPHERAL TESTS**, and then **FRONT PANEL**. See diagram below.




***Step 3.*** Follow instructions on the screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

***External Keyboard Interface Test***

This test verifies that the 373XXA external keyboard interface is functioning correctly.

***Equipment Required:***

An IBM compatible keyboard is required for this test.

***Procedure:***

***Step 1.*** Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

***Step 2.*** Select **DIAGNOSTICS** from menu; then in sequence select: **PERIPHERAL TESTS**, and then **EXTERNAL KEY-BOARD**. See diagram above.

***Step 3.*** Follow instructions on the screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

***Printer Interface Test***

This test verifies that the 373XXA printer interface is functioning correctly.

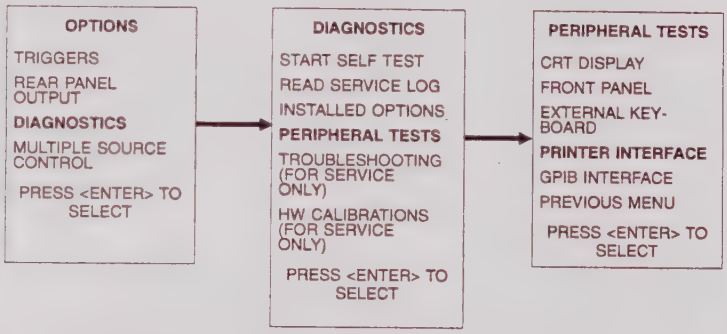
***Equipment Required:***

Printer Test Fixture (ANRITSU PN: B39553)

***Procedure:***

***Step 1.*** Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

***Step 2.*** Select **DIAGNOSTICS** from menu; then in sequence select: **PERIPHERAL TESTS**, and then **PRINTER INTERFACE**. See diagram below.




***Step 3.*** Follow instructions on the screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

### *GPIB Interface Test*

This test verifies that the 373XXA printer interface is functioning correctly.

***Equipment Required:***

GPIB cable (ANRITSU PN: 2100-2), or equivalent

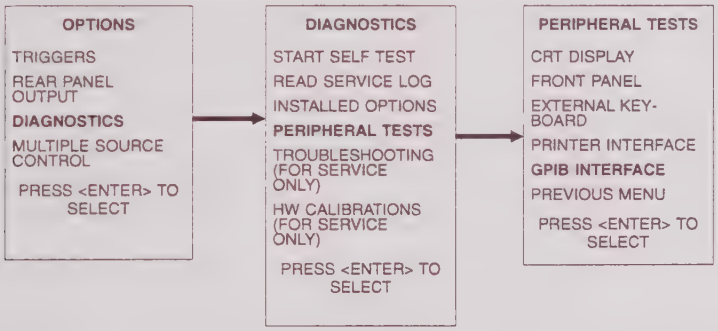
***CAUTION***

Insure that no other cables are connected to either of the two rear panel GPIB ports when performing this test.

***Procedure:***

***Step 1.*** Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

***Step 2.*** Select **DIAGNOSTICS** from menu; then in sequence select: **PERIPHERAL TESTS**, and then **GPIB INTERFACE**. See diagram below.




***Step 3.*** Follow instructions on the screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

## 3-5 SIGNAL PATH

These are a series of automated tests designed to insure the 373XXA internal signal paths are functioning properly and are capable of supporting stable calibrations and measurements. These test are performed using a software test program and an external computer/controller.

The test software performs the following operations and tests:

- Service Log Check
- Self Test
- Basic Sweep Operation and Speed Test
- High Level Noise Test
- System Stability Test
- RF Power Generation and Control Test
- Step Attenuators Accuracy and Repeatability Test
- Video IF Bandwidth Filters Operation Test
- Sampler Efficiency and Stability Test
- LO1/LO2 Linearity Test
- Source FM/Lock Signal Linearity Test

***Equipment required:***

37XXX Test Software (ANRITSU PN: 2300-178)

External computer/controller; refer to Table 1-1 located on page 1-9.

GPIB cable (ANRITSU PN: 2100-2), or equivalent

***Procedure:***

***Step 1.*** Refer to file "Readme.txt" of the distribution disk for information regarding setup of the computer/controller.

***Step 2.*** Using the GPIB cable, connect the external computer/controller to the IEEE 488.2 GPIB Interface port on the 373XXA rear panel.

***Step 3.*** Program may be run from floppy disk or copied to any folder in the computer and run from there.

***Step 4.*** Peform Non-Ratio and Transmission tests.

If any tests fail, refer to the Troubleshooting and Help selections of the Test Software menu for assistance.

# *Chapter 4*
# *Performance Verification*

## *Table of Contents*


| | | |
|---|---|---|
| 4-1 | INTRODUCTION | 4-3 |
| 4-2 | CALIBRATION AND MEASUREMENT CONDITIONS | 4-3 |
| | Standard Conditions | 4-3 |
| | Special Precautions: | 4-4 |
| 4-3 | MEASUREMENT ACCURACY | 4-4 |
| | Verification Software | 4-4 |
| | Verification Result Determination | 4-5 |
| 4-4 | VERIFICATION PROCEDURE | 4-5 |
| 4-5 | KEY SYSTEM PARAMETERS | 4-6 |
| | Measurement Environment Considerations | 4-6 |
| | Measurement Technique | 4-7 |

# Chapter 4
# Performance Verification

## 4-1 INTRODUCTION

This chapter provides specific procedures to be used to verify that the 373XXA is making accurate, traceable S-parameter measurements. You should perform the verification procedures in paragraph 4-3, "Verifying Measurement Accuracy," at least once annually.

Additionally, this chapter includes procedures that may be used to measure the following key system performance parameters:

- Effective Source Match
- Effective Directivity
- System Dynamic Range
- Frequency Accuracy
- Power Level Accuracy

The Operational Tests described in Chapter 3 should be performed prior to verifying system performance.

Please ensure you have read and fully understand the servicing concepts for the 373XXA presented in Chapter 1 prior to continuing with this chapter.

## 4-2 CALIBRATION AND MEASUREMENT CONDITIONS

Extremes in the surrounding environmental conditions and the condition and stability of the test port connectors, through-cable, and calibration kit determine system measurement integrity to a large extent.

These are all user controlled conditions, and as such, should be evaluated periodically for impact on system performance. If these conditions vary significantly with time, the system verification procedures should be performed more often than the recommended annual cycle.

### *Standard Conditions*

The standard conditions specified below must be observed when performing any of the operations in this chapter — both during calibration and during measurement.

Warm-up Time: One hour minimum.

Environmental Conditions:
Temperature: 23 +/- 3 deg C
Relative Humidity: 20-50% recommended.

Error Correction:

Perform software-guided 12 term calibration.

***Special Precautions:*** When performing the procedures in this chapter, observe the following precautions:

- Minimize vibration and movement of system and attached components and through-cable.
- Clean and check pin depth and condition of all adapters, through-cable(s), and calibration components.
- Pre-shape the through-cable(s) so as to minimize its movement during calibration and measurement activities.
- Ensure the system remains motion free in stable environmental conditions as defined above throughout warm-up, calibration, and measurement activities.

## 4-3 MEASUREMENT ACCURACY

The verification procedures described in the following paragraphs verify the published measurement accuracy and measurement traceability* for the 373XXA.

***Verification Software*** These procedures use the ANRITSU VNA Verification Software, PN: 2300-237, and the NIST traceable impedance transfer standards contained in the appropriate ANRITSU Verification Kit. The Standard Conditions and Special Precautions described in paragraph 4-2 should be observed when performing these procedures.

The appropriate ANRITSU Verification Kit to be used for performing these procedures is model dependent, as follows:

- Models 37317A and below, with Opt 7A: Verification Kit 3667
- All Models using K Connector test ports: Verification Kit 3668
- Models 37397A: Verification Kit 3669B

The impedance transfer standards contained in these kits are:

- 20 dB Attenuation Standard
- 50 dB Attenuation Standard
- 50 Ohm Air Line Standard
- 25 Ohm Mismatch (Beatty) Standard

The verification software performs the following functions:

- It guides the user through a full 12 Term calibration of the 373XXA.
- It guides the user through the measurement of the S-parameters of the NIST traceable impedance transfer standards (below).
- It verifies the measured values are within the specified measurement uncertainty limits.
- It indicates the pass/fail status of the measurements on the CRT display. It can also provide a hard copy printout of the measured

* Traceability to the U.S. National Institute of Standards and Technology (NIST)

data, measurement uncertainties, and the impedance transfer standards used.

***NOTE***

The total verification uncertainty in these 373XXA measurements includes the measurement uncertainty of the verification standards and the 373XXA measurement uncertainty.

***Verification Result Determination***

The software verification process compares the measured S-parameter data of the impedance transfer standards against the original standard data for those devices that was obtained using the Factory Standard 360 Vector Network Analyzer System (at ANRITSU). The factory Standard 360 system is traceable to NIST through the ANRITSU Calibration Laboratory's Impedance Standards. These standards are traceable to NIST through precision mechanical measurements, NIST approved microwave theory impedance derivation methods, and electrical impedance comparison measurements.

The quality of the verification results is very dependent on the degree of care taken by the user in maintaining, calibrating, and using the system. The most critical factors are:

- The stability and quality of the devices in the calibration and verification kits.
- The condition of 373XXA test port connectors and through-cables.
- The pin depths of all connectors, and the proper torquing of connections. These same factors also affect 373XXA measurement quality.

Consult the Operating Manuals supplied with the ANRITSU Calibration and Verification Kits for proper use, care, and maintenance of the devices contained in these kits.

## 4-4 VERIFICATION PROCEDURE

The performance verification procedure for the ANRITSU 373XXA VNA is described below. Refer also to the Model 360X/37XXX VNA Performance Verification Software Users Guide, P/N: 10410-00162, which is located in Appendix E at the rear of this manual. This Software Users Guide explains in detail the procedures to be used for the installation and operation of the Verification Software on your computer/controller.

***Equipment required:***

ANRITSU 37300A Verification Software, PN: 2300-237 (Version 3.1 or above of 2300-237 software is necessary to verify the 37397A).

External computer/controller; refer to Table 1-1 located on page 1-9.

ANRITSU Verification Kit appropriate for the 373XXA model; refer to paragraph 4-3.

GPIB cable (ANRITSU PN: 2100-2), or equivalent

***Procedure:***

***Step 1.*** Using the GPIB cable, connect the external computer/controller to the IEEE 488.2 GPIB Interface port on the 373XXA rear panel.

***Step 2.*** Insert the CD ROM into its drive and install the 2300-237 software.

***Step 3.*** Follow the directions displayed on the computer screen to perform all tests.

If the calibration fails, check the connectors of the calibration kit devices and the impedance transfer standards for damage, cleanliness, and proper connection and torquing. These are the most common causes for verification failures.

If the problem persists, check system Directivity, Match, and Dynamic Range, as described in the next paragraph.

## 4-5 KEY SYSTEM PARAMETERS

The following paragraphs describe procedures for automated measurement of the key system performance parameters listed below. Measurement of these parameters is not required for system verification; however, it is highly recommended to ensure that the complete 373XXA measurement environment is stable and capable of supporting accurate measurements.

- Effective Source Match
- Effective Directivity
- System Dynamic Range
- Frequency Accuracy
- Power Level Accuracy

### *Measurement Environment Considerations*

As with the verification procedures, the quality of the measurement of the system performance parameters listed above is very dependent on the measurement environment.

The complete 373XXA measurement environment consists of:

- Condition and stability of the test ports, through-cable, and calibration kit mating connectors.
- Settings and stability of the surrounding environment, especially temperature, humidity, and vibration. To maintain the highest system performance, avoid changing these conditions, especially tem-

perature, during warm-up, calibration, and when making measurements on your DUT.

- The use of proper microwave connector mating techniques.

***Measurement Technique***

The measurements of the key system performance parameters are performed using the ANRITSU 37XXX Test Software, PN: 2300-178.

***NOTE***

The Standard Conditions and Special Precautions described in paragraph 4-2 should be observed when performing these measurements.

The software will use the following standards to determine system performance values:

- Assurance Air Line Set
- Offset Termination
- Frequency Counter
- Power Meter

***Equipment required:***

37XXX Test Software (ANRITSU PN: 2300-178)

External computer/controller; refer to Table 1-1 located on page 1-9.

GPIB cable (ANRITSU PN: 2100-2), or equivalent

***Measurement Procedure:***

***Step 1.*** Refer to file "Readme.txt" of the distribution disk for information regarding setup of the computer/controller.

***Step 2.*** Using the GPIB cable, connect the external computer/controller to the the 373XXA IEEE 488.2 GPIB rear panel connector.

***Step 3.*** Program may be run from floppy disk or copied to any folder in the computer and run from there.

***Step 4.*** Follow the directions displayed on the computer screen to perform all tests.

***NOTE***

Some tests require that the first test selected *must* be the 12-Term Calibration. The software will guide you through this calibration.

If any tests fail, refer to the Troubleshooting and Help selections of the Test Software menu for assistance.

# *Chapter 5*
# *Troubleshooting*

## *Table of Contents*


| | | |
|---|---|---|
| 5-1 | INTRODUCTION | 5-3 |
| 5-2 | ASSOCIATED INFORMATION IN THIS MANUAL | 5-3 |
| 5-3 | RECOMMENDED TEST EQUIPMENT | 5-4 |
| 5-4 | SYSTEM DOES NOT POWER-UP | 5-4 |
| | Line Source and Interface Checks | 5-4 |
| | Power Supply Voltages Check | 5-4 |
| | Power Supply Module Check | 5-6 |
| 5-5 | SYSTEM DOES NOT BOOT-UP | 5-7 |
| | Boot-up Process Sequence | 5-7 |
| | Troubleshooting Boot-up Problems | 5-8 |
| | Hard Disk Problem 1 | 5-8 |
| | Hard Disk Problem 2 | 5-9 |
| | Floppy Disk Problems | 5-9 |
| | Screen Display Problems | 5-10 |
| 5-6 | SYSTEM HAS ERROR CODE | 5-10 |
| | Phase Lock Error Codes (6000 Series) | 5-11 |
| | Service Log Snap Shot Data | 5-12 |
| 5-7 | SOURCE/TEST SET/RECEIVER | 5-17 |
| | Signal Source Phase Lock Loop Assemblies | 5-17 |
| | Signal Source/Test Set Module Error Codes | 5-18 |
| | Isolation Procedures | 5-19 |
| 5-8 | PERIPHERALS/ INTERFACE | 5-21 |
| | CRT Display Test Failures: | 5-21 |
| | Front Panel Test Failures: | 5-22 |
| | External Keyboard Interface Test Failures: | 5-22 |
| | Printer Interface Test Failures: | 5-22 |
| | GPIB Interface Test Failures: | 5-22 |
| 5-9 | MEASUREMENT IN QUESTION | 5-22 |
| | Measurement Conditions Check List | 5-23 |

Many of the troubleshooting procedures presented in this chapter require the removal of instrument covers to gain access to printed circuit assemblies and other major assemblies.

***WARNING***

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

***CAUTION***

Many assemblies in the 373XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

***CAUTION***

Never operate the 373XXA with connector J3 of the A21A2 Source Control PCB disconnected. Operation in this mode may cause damage the A31 Buffer Amplifier/Sampler assembly.

# *Chapter 5*
# *Troubleshooting*

## 5-1 INTRODUCTION

This chapter provides specific procedures to be followed when troubleshooting 373XXA VNA systems. While performing these procedures, always observe the warnings and cautions on the opposite page.

To use the troubleshooting procedures in this chapter:

1. Select the paragraph heading (starting with paragraph 5-4) that best describes the nature of the 373XXA VNA system fault. Refer to the Table of Contents page.

2. Perform the procedure contained in the selected paragraph. In general, the steps within each procedure should be followed in the order presented.

3. When removing and replacing the various assemblies and components specified by the troubleshooting procedures in this chapter, refer to Chapter 8, Remove and Replace Procedures, as necessary.

4. If a step cannot be successfully completed, stop; correct the immediate problem, and then continue on to the next step until all the appropriate steps in the procedure are completed.

5. After troubleshooting and correcting a problem, perform the procedures in Chapter 3, (Operational Tests) and Chapter 4 (Performance Verification), as appropriate. This should be done to insure that the system has been fully and correctly restored to proper operation.

The procedures described in this chapter provide a general approach to troubleshooting 373XXA VNA problems. They are particularly useful for problems where the 373XXA is only partially functional. The Internal Diagnostic Menus described in Appendix A are very useful for evaluating 373XXA system performance. They may be used alone, or in conjunction with the procedures in this chapter.

Please ensure you have read and fully understand the servicing concepts for the 373XXA presented in Chapter 1 prior to continuing with this chapter.

## 5-2 ASSOCIATED INFORMATION IN THIS MANUAL

While using the troubleshooting procedures in this chapter, refer also the the following information:

- Appendix A, Diagnostics Menus, fully describes the 373XXA Diagnostics menu tree, including the SERVICE LOG menu.
- Appendix B, Error Codes and Messages, for details on each of the 373XXA hardware related error messages.
- Chapter 6, System Description, for a brief technical description of the 373XXA VNA system operation.

## 5-3 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for the troubleshooting procedures presented in this chapter is listed in Chapter 1, Table 1-1 (page 1-9).

## 5-4 SYSTEM DOES NOT POWER-UP

If the 373XXA does not power-up when connected to a source of AC power and the Power key is pressed, perform the power supply checks described below.

***WARNING***

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

***Line Source and Interface Checks***

Check as follows:

Step 1. Verify that the AC power source is providing stable power at the correct line voltage.

***NOTE***

The 373XXA is designed to automatically sense and operate with AC power line voltages in the range of 85 - 240 VAC, with a frequency of 48 - 63 Hz (540 VA maximum).

Step 2. Verify that the power input cord is in good condition.

Step 3. ensure that the system power line fuse is installed, that it is not open, and that it is the correct value (8 A, Slow Blow).

***Power Supply Voltages Check***

Verify that the 373XXA power supply voltages are correct as follows:

Step 1. Press the 373XXA Power key **off**, and and disconnect the power input cord from the 373XXA. ensure all external connections to the system front and rear panel are also disconnected.

Step 2. Remove bottom panel, and lay the system down on its left (monitor) side. Refer to Chapter 8, Remove and Replace Procedures.

Step 3. Reconnect the power line input cord to the system and Press the 373XXA Power key **on**.

Step 4. Using a DMM or an oscilloscope, measure the DC power supply voltages listed in Table 5-1. Connect the DMM/oscilloscope to the top of the cable connectors at J13 and J4 on the Motherboard (A17). Refer to Figure 5-1 and Table 5-1.

***Table 5-1.*** *373XXA DC Power Supply Voltage Checks*

| Connect To: | | | DC Supply Voltage | | AC Ripple and Noise |
|---|---|---|---|---|---|
| Conn | Com (Pin) | Meas (Pin) | | | |
| J13 | 8 | 16 | 0 Vdc | | 50 mVpp |
| J13 | 8 | 1 | +4.8 Vdc | +1% / –0% | 50 mVpp |
| J4 | 4 | 1 | +9 Vdc | +5% / –0% | 100 mVpp |
| J4 | 4 | 6 | +18 Vdc | +10% / –0% | 100 mVpp |
| J4 | 4 | 10 | –18 Vdc | +10% / –0% | 100 mVpp |
| J4 | 4 | 12 | +27 Vdc | +5% / –0% | 100 mVpp |
| J4 | 4 | 14 | –27 Vdc | +5% / –0% | 100 mVpp |

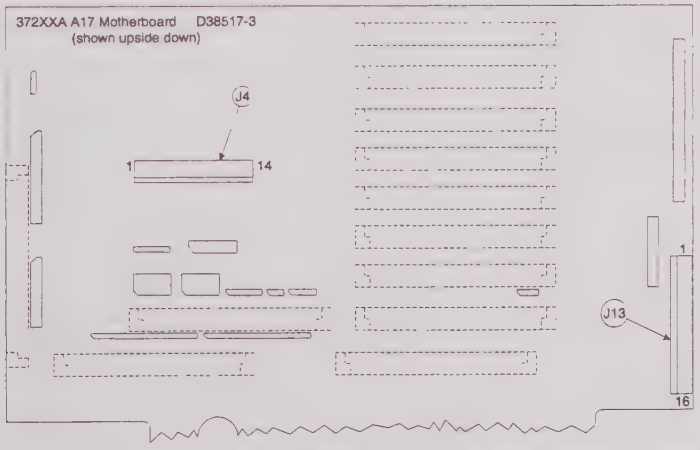



**Figure 5-1.** *Location of Connectors for Power Supply Voltage Checks*

Step 5. Connect the common lead of the oscilloscope to J13, pin 8. Measure the Power Supply Sync signal (PS_SYNC) on J13, pin 14:

*Specification:* 2-4 vpp Sine Wave at 109.89 KHz

***NOTE***

The power supply module will power-up without the PS_SYNC signal being present. However, the lack of this signal will introduce signal purity problems when the system is performing measurements.

***Power Supply Module Check***

If any of the DC voltage tests fail, verify that the power supply module is operating properly with minimal impact from the system as described in the procedures below.

***NOTE***

If a power supply voltage is low, it may be due to excessive current draw from the system and not a fault in the power supply.

Steps 1 through 4 verify the operation of the + 9, ±18, and ±27 Vdc supplies:

Step 1. Press the 373XXA Power key **off**, and and disconnect the power input cord.

Step 2. Disconnect the power supply module from the A17 Motherboard at J4.

Step 3. Reconnect the power line input cord to the system and press the 373XXA Power key **on**.

Step 4. Using a DMM and/or an oscilloscope, measure the power supply voltages at the power supply connector pins that correspond to the Motherboard pins for the + 9, ±18, and ±27 Vdc supplies. Refer to Table 5-1 and Figure 5-1 (previous page).

Steps 5 through 8 check the +5 volt supply. This power supply requires at least a 10% load to turn on. Therefore, at least one of the digital PCBs A9, A13, or A14 (which use the 5 volt supply) must be installed in the system during this procedure.

Step 5. Press the 373XXA Power key **off**, and reconnect the power supply module to the Motherboard at J4.

Step 6. Unplug digital PCB's A13 and A14.

Step 7. Press the 373XXA Power key **on**.

Step 8. Using a DMM and/or an oscilloscope, measure the +5 volt power supply at connector J13 on the Motherboard. Refer to Figure 5-1 and Table 5-1, (page 505).

Step 9. Press the 373XXA Power key **off**, and and reinstall the A13 and A14 PCB's removed in Step 6.

If any of the DC voltage tests fail in steps 1 through 8 above, replace the power supply module.

If any of the DC voltage tests fail with the power supply module connected to the 373XXA Motherboard — but pass with it disconnected — then the most probable cause of the failure is that one of the 373XXA assemblies is demanding an excessive amount of current. To locate the failed assembly:

1. Press the 373XXA Power key **off**, and unplug a single assembly.

2. Press the 373XXA Power key **on**, and note if the failed power supply functions normally.

3. Repeat Steps 1 and 2 until an assembly is found that clears the power supply failure. The removed assembly is suspect and should be replaced.

## 5-5 SYSTEM DOES NOT BOOT-UP

If the 373XXA does not boot-up when it is powered-up, perform the checks described below.

### *Boot-up Process Sequence*

The boot-up process is controlled by the firmware located on the A9 PCB assembly (processor PROM) The boot-up activities include:

- Testing and initializing the A9 Main Processor PCB
- Testing communication between the A9 PCB and the digital PCB assemblies (A13, A14, A15, A16). The following messages will be displayed at this juncture:
  - Initializing front panel knob (A14/A20)....
  - Initializing GPIB (A13/A18)....
  - Initializing external keyboard (A13)....
  - Initializing external trigger (A13/A5)....
  - Initializing front panel (A14/A20)....
- Loading of system software from disk into memory
- Starting operation of the system software.
- System is booting—message is displayed.

At this point, the system software continues the boot-up process by performing the following activities:

- Issues command to A15 PCB to change display from TEXT mode to GRAPHIC mode and display ANRITSU logo.
- Performs basic communication tests between the digital system (A13, etc.) and the analog subsystem (A1-A8, A21A1, A21A2); this is part of a minimal self test.
- Conducts an IF Calibration
- Resets and loads the front panel state that was in effect prior to the last power down
- Starts the measurement process

***NOTE***

The system software fully controls the 373XXA VNA system after boot-up (with operator intervention and guidance). The system software is only loaded once upon initial power up.

***Troubleshooting Boot-up Problems***

To start the troubleshooting of boot-up related problems, perform the following preliminary checks:

1. Note any error messages displayed on the CRT display during the boot-up process.
2. Observe the front panel and the display during the boot-up process for information as to which part of the process failed or did not execute.
3. Verify that the system power supplies are working properly as per paragraph 5-4, above. Note particularly the operation of power supplies immediately after power-up.
4. Try to boot the instrument from the floppy disk and repeat steps 1 and 2 above.

Upon completion of the preliminary checks (above), perform the following procedures, as appropriate.

***Hard Disk Problem 1***

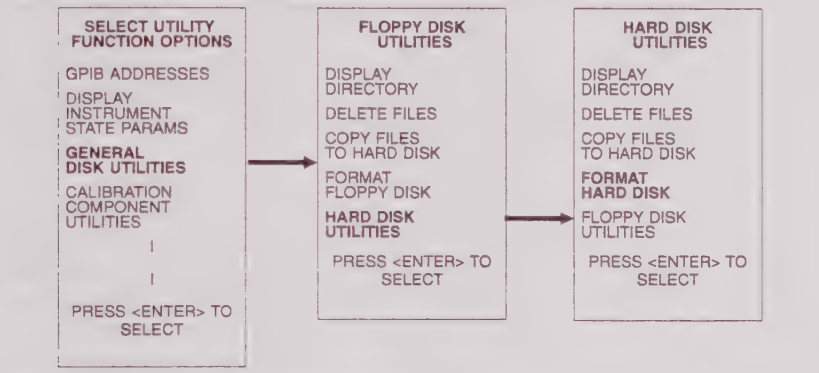
If a hard disk problem is indicated during bootup from a floppy disk, but the system can bootup correctly from the hard disk:

Step 1. Boot up from the hard disk, then format the Hard Disk using the procedure below.

***CAUTION***

Formatting the hard disk will erase all files on the hard disk. Before starting the disk formatting process, copy any files you wish to save to a floppy disk.

Step 2. Press the Utility Menu key (System State key group) to display the **UTILITY FUNCTIONS OPTIONS** menu. From menu, select **GENERAL DISK UTILITIES** (see below).




Step 3. If **FLOPPY DISK UTILITIES** menu appears, select **HARD DISK UTILITIES**.

Step 4. From **HARD DISK UTILITIES** menu, select **FORMAT HARD DISK**.

Step 5. After formatting is complete, reload System Software from the master floppy diskettes. Retry boot-up. If fail, contact ANRITSU Customer Service Center.

***Hard Disk Problem 2*** If system does not bootup from hard disk and floppy disk:

Step 1. When the five initializing messages are displayed after power on, press any key within 2 seconds.

Step 2. Follow the instruction on the display to format the hard drive. After formatting is complete, reinstall system software from the master floppy diskettes. Retry boot-up.

Step 3. If fails, replace the A16 Hard Disk PCB; reinstall system software from the master floppy diskettes.

Step 4. Retry boot-up. If fail, contact ANRITSU Customer Service Center.

***Floppy Disk Problems*** If a floppy disk problem is indicated during bootup from floppy disk but the system is able to bootup from the hard disk:

Step 1. Ensure the floppy disk media is in good condition

Step 2. Verify disk drive connection at Motherboard connector J2.

Step 3. Retry boot-up. If fail, replace the A13 - I/O#1 PCB.

Step 4. Retry boot-up. If fail, replace the Floppy Disk Drive.

***Screen Display Problems***

If the 373XXA system appears to have no screen display, perform the preliminary check below and then perform checks 1 - 3, as appropriate:

*Preliminary Check* - Press the 373XXA Power key **off** and then **on** several times. Each time power is reapplied, pause and wait for the 373XXA software system to boot-up. During boot-up, observe the top left hand portion of the CRT display.

***NOTE***

An alternative method to reset and re-boot the software system is to press the red button on the A9 Main Processor PCB. Observe the messages displayed on the screen during the boot-up process. Verify that the following messages are present :

- Initializing front panel knob (A14/A20)....
- Initializing GPIB (A13/A18)....
- Initializing external keyboard (A13)....
- Initializing external trigger (A13/A5)....

*Check 1:* If during boot-up the 373XXA does not attempt to display any messages at all, proceed as follows:

Step 1. Replace the A15 Graphics Processor PCB.

Step 2. Retry boot-up. If fail, replace the Internal VGA Monitor.

Step 3. Retry boot-up. If fail, replace the A9, Main Processor PCB.

Step 4. Retry boot-up. If fail, contact ANRITSU Customer Service Center.

*Check 2:* If the system halts before it completes all five digital sections, process as follows:

Step 1. Replace the PCB indicated on the last displayed message. Example: If the system halt at the "Initializing front panel knob (A14/A20)....," replace the A14 and A20 PCBs.

Step 2. Retry to boot the system. If it still fails, contact ANRITSU Customer Service.

## 5-6 SYSTEM HAS ERROR CODE

If the 373XXA detects a problem during normal operation, an error message consisting of an error code followed by a brief error message will be displayed on the screen. The error code will also be written to the service log along with some of the operating data gathered from the system at the time of failure.

System error codes in the range 0100 - 3999 identify the suspected failed subassembly in the two most-significant digits of the error code. For example: error codes 0200 - 0299 are related to the A2, LO2 PCB assembly. This error code assignment scheme allows for quick identification of suspect assemblies.

***NOTE***

Refer to Appendix B, Error Codes/Messages, for a list of the error codes/messages for 37300A VNA systems.

There are cases when a fault on one assembly will cause a different assembly to be identified as faulty (per the error code designated). This happens when a failure occurs on an assembly that provides a stimulus or a calibration signal to other assemblies in the system. Example: the A7 LO3 PCB provides the IF Calibration signal to the A3, A4, and A6 PCB's. If the IF Cal signal is faulty, error codes will be reported for the A3, A4, A6, and A7 PCB's.

***NOTE***

An aide to troubleshooting system failures using error codes is a good understanding of system and subassembly operation. Refer to the descriptions of system and subassembly operation and block diagrams located in Chapter 7, System Description.

***Self TestError Codes***

Error codes 0100 - 3999, with few exceptions, are produced as a result of a failure when the system self test is run. These error codes will **not** be displayed on the CRT screen. Only the overall result of the self test (PASS/FAIL) will be displayed at the conclusion of the self test. However, any error codes due to the self test will be written to the service log as the self test is executed.

***NOTE***

The exceptions are error codes with 00 in the two least-significant digits, for example: 0500 A/D CONVERSION FAIL. These errors are produced at run time if a problem is encountered when the system is actively making measurements.

***Phase Lock Error Codes (6000 Series)***

The Phase Lock error codes (6000 - 6999) will have an alphabetical suffix (code) following the message. For example: 6079 PHS LCK FAIL ABCDG. This code consists of one or more letters from A - G that represent the sub assembly that was not locked and/or the nature of the failure. The phase lock failure mode suffixes are listed in Table 5-2.

Note that most phase lock error codes will normally consist of a letter identifying the unlocked assembly and the **D** and/or **DE** letters that indicate the Source Module is also unlocked. This is normal since all components in the phase lock loop must be correctly locked in order for

*Table 5-2. Phase Lock Error Message Failure Suffixes*

| Failure Suffix | Failed Assembly/ Failure Mode | Failure Suffix | Failed Assembly/ Failure Mode |
|---|---|---|---|
| A | 10 MHz not present | E | IF lock signal level too low |
| B | L01 unlocked | F | Ext synthesizer unlocked |
| C | L02 unlocked | G | L03 unlocked |
| D | Source unlocked | none | Unknown |

the Source Module to achieve lock. Refer to Figure 5-2 for a flowchart that troubleshoots the >40 GHz models (37397A).

Example 1: Any of the following error messages indicate that the LO1 PCB assembly was not able to lock:

```
6002 PHS LCK FAIL B
6010 PHS LCK FAIL BD
6026 PHS LCK FAIL BDE
```

Also note that if the 10 MHz Reference fails, depending on the failure, the system will not be able to lock any of the phase lock loop components: A1, A2, A7, A8, or Source Module.

Example 2: Either of the following error messages indicate a 10 MHz Reference problem:

```
6001 PHS LCK A
6015 PHS LCK ABCDG
```

***Service Log Snap Shot Data***

Error codes will be written to the service log along with some data representing a "Snap Shot" of system conditions at the time of failure. Usually, the data included in the snap shot helps to provide faster diagnosis of the error condition. The common snap shot data items that will be useful inassembly level troubleshooting and fault diagnosis efforts are listed in Table 5-3.

***NOTE***

Some of the data included in the snap shot is useful only for factory troubleshooting activities.

*Table 5-3. Service Log Snap Shot Data Items*

| Item | Description |
|---|---|
| SWP | Sweep direction:<br>F = forward (S11, S21), R = reverse (S22, S12) |
| PWR | System source power setting |
| SYS | System frequency setting |
| A | The calibration results for the Test A Channel PCB (A3): This is a series of 16 values divided into groups of four. Each group should have values that are approximately ¼ that of those in the previous group.<br><br>The first group data values should be approximately: 1.00 0.00 0.00 1.00. The values of the next group should be ¼ that of those values i.e., 0.25 0.00 0.00 0.25. The same applies for the values in the remaining two groups. |
| B | The calibration results for the Test B Channel PCB (A6). See description for "A" above. |
| R | The calibration results for the Reference A (or B) Channel PCB (A4). See description for "A" above. |
| *<OVL>* | Indicates the value was too far out of range to be measurable. |
| PHSLCK | Source Locking: L=Source Lock Mode, T=Tracking Mode, S=Set On Mode |

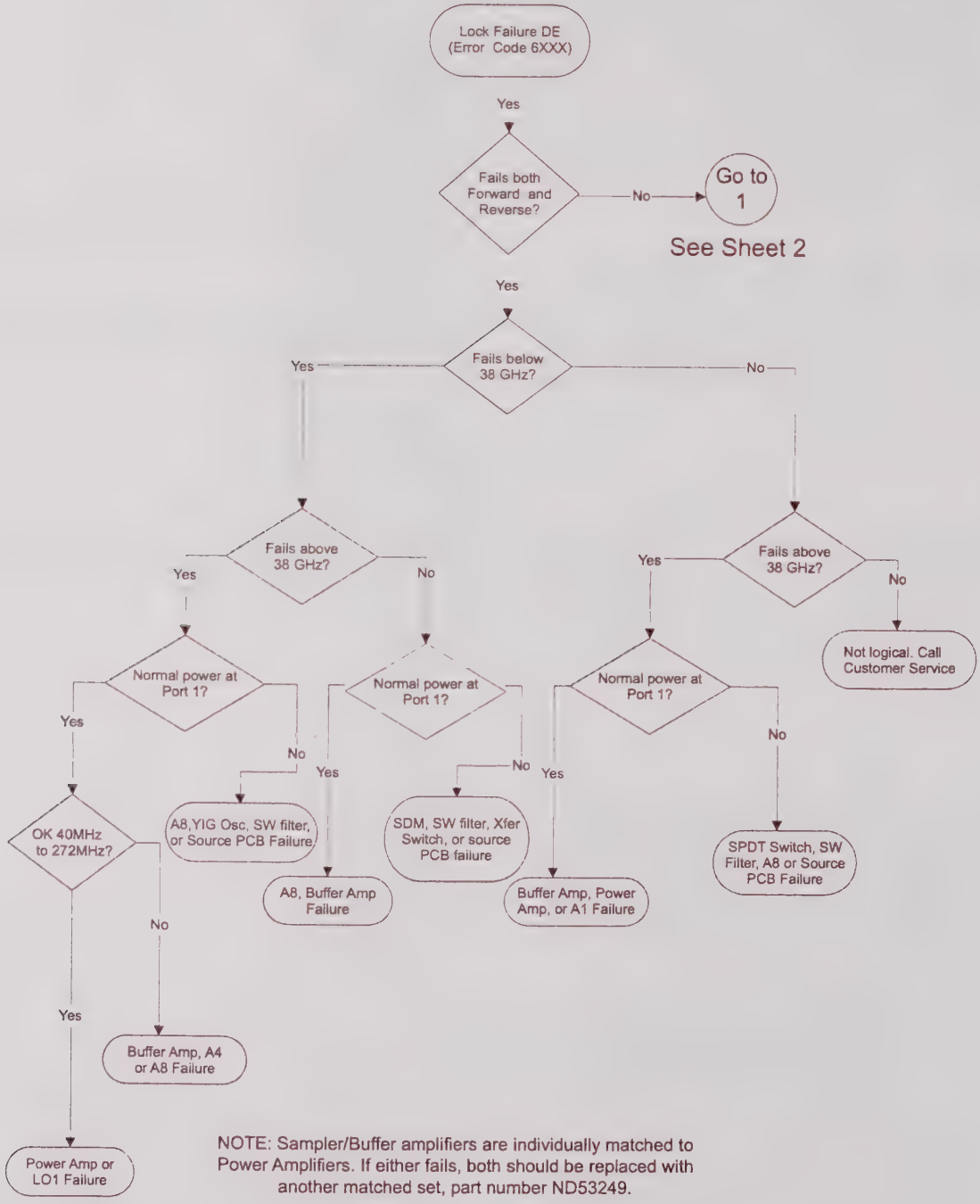



**Figure 5-2.** *Error Code DE Lock Failure Troubleshooting (37397A) (1 of 3)*

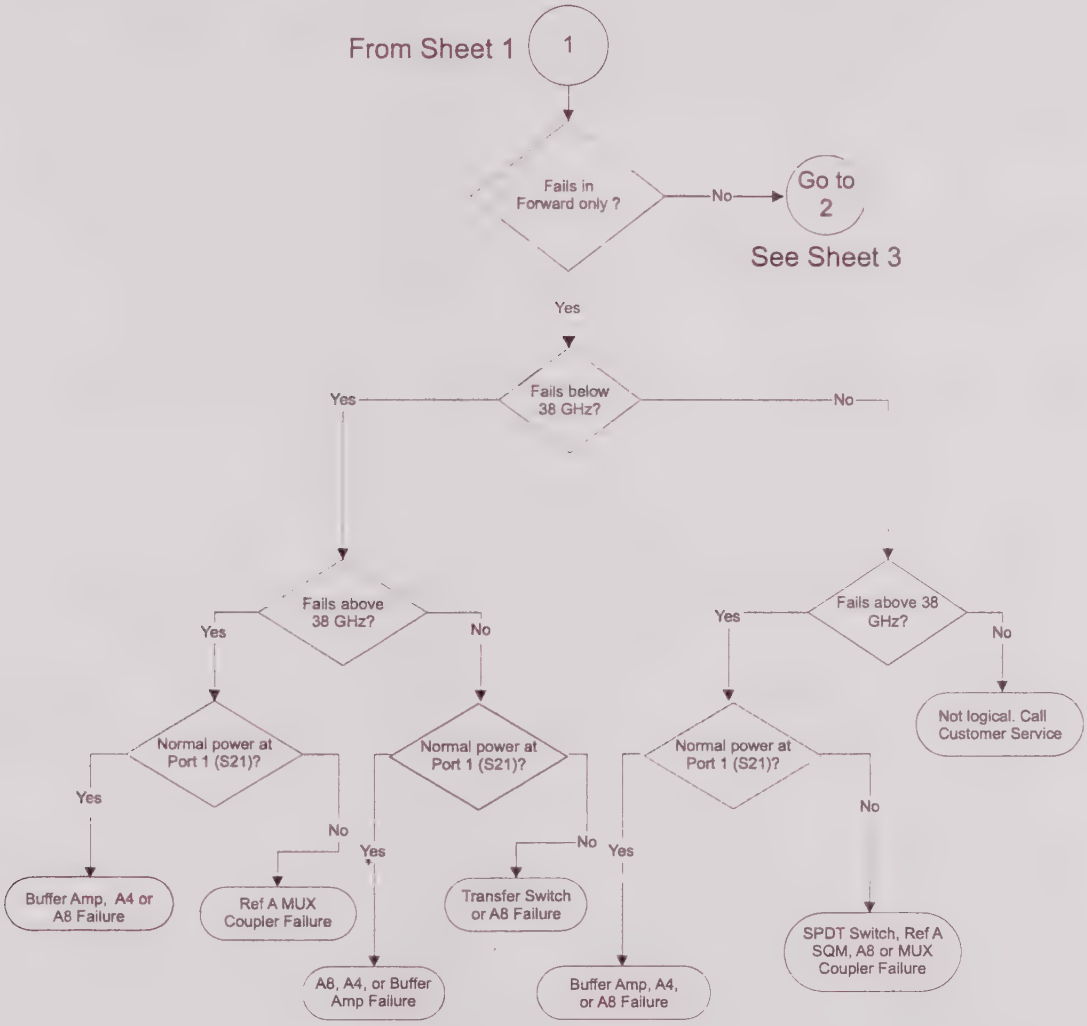



**Figure 5-2.** *Error Code DE Lock Failure Troubleshooting (37397A) (2 of 3)*

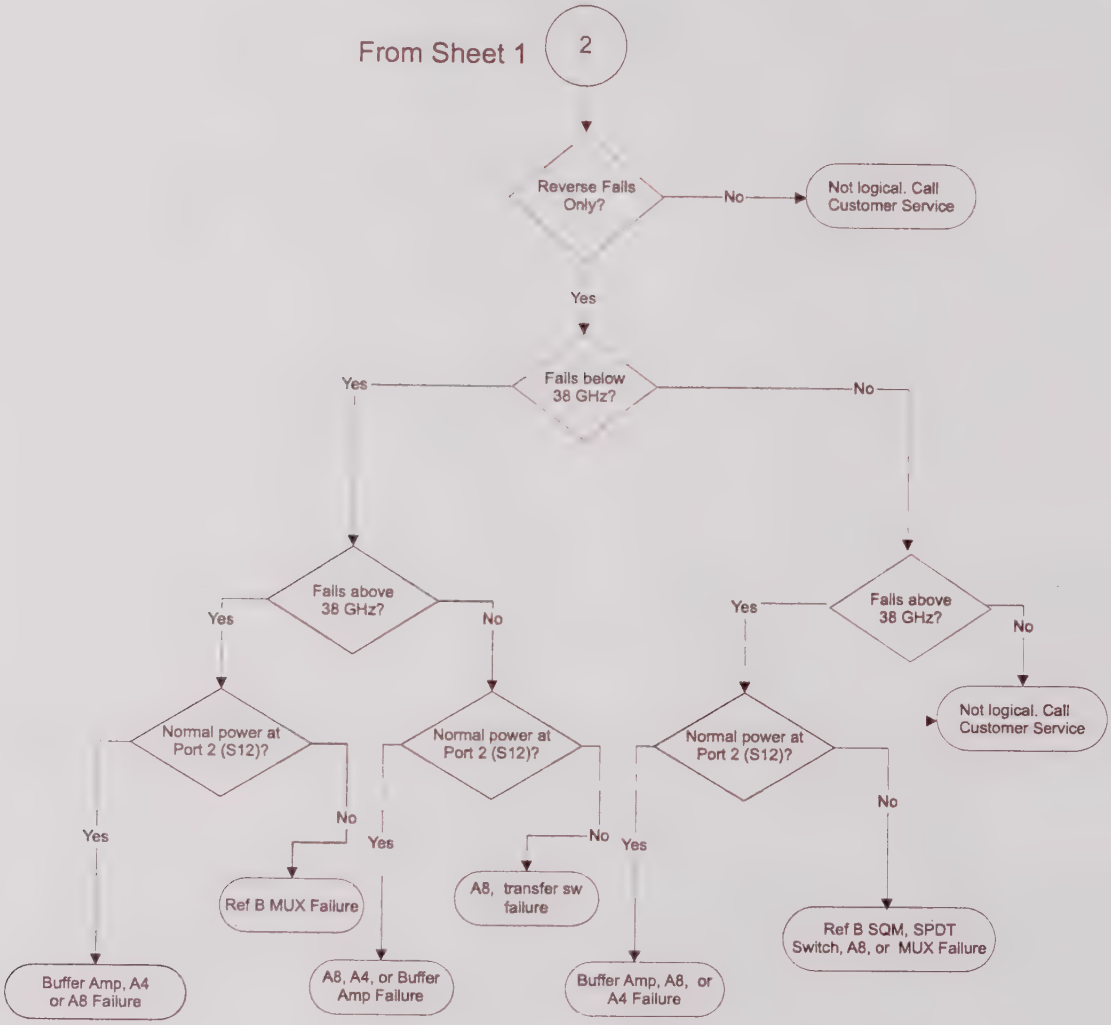



**Figure 5-2.** *Error Code DE Lock Failure Troubleshooting (37397A) (3 of 3)*

## 5-7 SOURCE/TEST SET/RECEIVER

Because of the 373XXA phase-lock loop structure, it is not easy to distinguish between failures that occur in the Source Module, the Test Set Module and the Receiver Module. In order to troubleshoot failures occurring in this group of modules, it is essential to be familiar with how each module functions and how it interacts with the other modules. Refer to Chapter 7, System description, for a functional description of each module.

For Model 37397A, refer to Figure 5-3 and Figure 5-4 (rear of section) for aid in troubleshooting Test and Source Lock signal paths. Refer also to Table 5-6 (rear of section) for a list of typical reference signal values, and to Tables 5-7 and -8 for Transfer and DPDT Switch Voltages.

### *Signal Source Phase Lock Loop Assemblies*

The 373XXA assemblies that contain circuits that are part of the signal source phase-lock loop (Source Lock function) are listed in Table 5-4.

***Table 5-4.*** *Phase Lock Loop Assemblies***

| Assemblies | Location |
|---|---|
| A21A1 Source YIG/Bias PCB | Source Module |
| A21A2 Source Control | Source Module |
| YIG Oscillator | Source Module |
| Switched Filter | Source Module |
| Down Converter | Source Module |
| Switched Doubler Module SDM* | Test Set Module |
| Transfer Switch | Test Set Module |
| Buffer Amplifier | Receiver Module |
| A1 LO1 PCB | Receiver Module |
| A2 LO2 PCB | Receiver Module |
| A4 Reference IF PCB | IF Section |
| A8 Source Lock/Signal Separation Control PCB | Analog Subsystem |
| A9 Main Processor PCB | Digital Subsystem |

* Model 37369A only, ** See Figure 5-4 for 37397A models

Failures occurring in the Source Module, Test Set Module and Receiver Module will generally cause the system to produce "Phase Lock Fail" error codes. Included with the Phase Lock Fail error codes are alphabetical suffixes that indicate the probable malfunctioned sub-assembly.

Example: **6008 PHS LCK FAIL D**

The letter "D" in the error code above indicates that the failure is possibly in the Source Module. (Refer to Table 5-3.)

***Signal Source/Test Set Module Error Codes***

Failures occurring in the Signal Source Module and Test Set Module will also produce the error codes listed in Table 5-5.

***Table 5-5.*** *Signal Source / Test Set Module Error Codes*

| Error Codes | Possible Failed Assemblies |
|---|---|
| 5110 RF PWR UNLEVELED | All components in Source Module and Test Set Module |
| 5210 REF A CHAN RF OVERLOAD | Transfer Switch |
| 5220 REF B CHAN RF OVERLOAD | Transfer Switch |
| 5230 TA CHAN RF OVERLOAD | Transfer Switch or A21A2 PCB |
| 5240 TB CHAN RF OVERLOAD | Transfer Switch or A21A2 PCB |

***Codes***

***NOTE***

The 373XXA has extensive built-in troubleshooting tools that are useful for troubleshooting the failures listed in Table 5-5. These and other troubleshooting tools are accessed from the Option Menu key, which is part of the enhancement keygroup. (From the select OPTIONS menu select **DIAGNOSTICS**, then select **TROUBLESHOOTING**). Refer to Appendix A.

Troubleshooting tools that are available from the TROUBLESHOOTING menu that are useful for locating faults occurring in the Source Module, Test Set Module and Receiver Module are:

***NOTE***

The troubleshooting tools listed below are used to test the 373XXA to factory set limits when the ANRITSU 37300A Test Software (2300-178) is run.

When run from the TROUBLESHOOTING menu, not all tests will display limit lines (as is the case when the 37300A Test Software 2300-178 is used).

**NON-RATIO PARAMETERS**

This function displays the output of each of the individual test set channels. It is especially useful for verifying the performance of the Buffer Amplifier and Power Amplifier.

***NOTE***

A through-line cable connecting Port 1 and Port 2 is required for this check.

By examining these displays in conjunction with other failure symptoms, the failed assembly can be located.

*Example:* Suppose the Non-Ratio Parameter screen display shows power holes above 270 MHz on all traces and in both sweep directions. A possible cause for this condition is a failure of the Power Amplifier assembly at certain frequencies. (Refer to Analog Subsystem Block Diagram in Figure 7-2 on page 7-6).

**LO1**
This function allows user to verify whether the A1 LO1 PCB is operating properly.

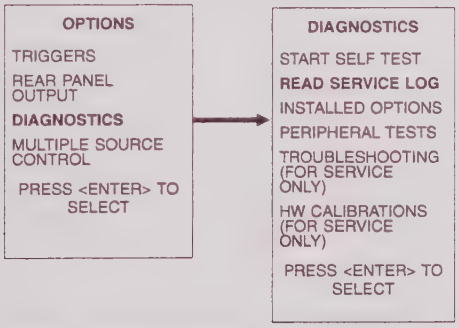
**LO2**
This function allows the user to verify whether the A2 LO2 PCB is operating properly.

**SOURCE**
This function allows the user to verify whether the Source Module is operating properly.

***Isolation Procedures*** The procedures in the following paragraphs will help you isolate the fault to the major assembly.

*Check #1* *Proceed as follows:*

Step 1. *Press Option Menu* key and select the **DIAGNOSTICS** menu option.




Step 2. Select the **READ SERVICE LOG** menu option to display the error entry associated with the system failure. Observe the snap shot data included as part of the error entry and note the sweep direction indication for each error code. (Refer to Table 5-3.)

Step 3. Determine whether the failure occurs during forward measurements (S11, S21) and/or reverse measurements (S22, S12):

If the problem occurs in both directions at all frequencies, the fault could be in the Receiver Module, Signal Source Module, or Test Set Module.

If the problem occurs in both directions at only certain frequencies, the fault could be in the Signal Source Module.

If the problem occurs in only one direction, the fault could be in the TEST SET MODULE.

Step 4. Run the 37XXX Test Software (2300-178) program to verify operation of the Buffer Amplifier, A1 LO1 PCB, A2 LO2 PCB, and Source control PCB.

Use the information obtained in steps 1 – 4 above to determine whether the failure occurs in the Source Module, Test Module or Receiver Module. Replace the suspected failed assembly, and perform any required adjustment(s). Then retest. If the 373XXA still fails, contact ANRITSU Customer Service Center for further assistance.

***NOTE***

To obtain technical service support from your nearest ANRITSU Customer Service Center, refer to Paragraph 1-8, Service Support Information.

*Check #2* If you have determined that the failure occurs in both sweep directions, only at certain frequencies, and that Error Code 5110 is recorded in the Service Log, use the following procedures to determine which assembly may have failed:

Step 1. Set the 373XXA Start and Stop frequencies for the following bands:

| Band | Start | Stop |
|---|---|---|
| 1 | 22.5*/40 MHz | 2.0 GHz |
| 2 | 2.0 GHz | Upper band-edge frequency for model. (20 GHz for 37369A) |
| 3 | 20.0 GHz | 40.0 GHz (for Model 37369A only) |

* Models 37311A and 37317A

Step 2. If the problem occurs in Band 1, replace the Down Converter assembly and repeat test.

If it fails, contact ANRITSU Customer Service Center.

Step 3. If the problem only occurs in Band 3, replace the Switched Doubler Module assembly and repeat test.

If it fails, replace Switched filter and repeat test.

If it fails, contact ANRITSU Customer Service Center.

Step 4. If the problem only occurs in Band 2, replace Switched Filter assembly and repeat test.

If it fails, contact ANRITSU Customer Service Center.

***NOTE***

After replacing a component, perform a Frequency Calibration and a RF power/ALC Calibration. Refer to Chapter 6, Adjustments.

*Check #3* If you have determined that failure occurs in both sweep directions, *at all frequencies* and Error Code 5110 is recorded in the Service Log, the failed component could be any of the following assemblies:

1. Transfer Switch
2. Switched Doubler Module
3. YIG Oscillator
4. A21A1 YIG Bias PCB
5. A21A2 Source Control PCB

Replace the components listed above in sequence. After each replacement recalibrate unit (see note above) and retest. If 373XXA still fails, contact your nearest ANRITSU Customer Service Center.

## 5-8 PERIPHERALS/ INTERFACE

The following paragraphs contain procedures to be used for troubleshooting 373XXA peripheral or interface test failures. Select the paragraph subheading that corresponds to the test that failed.

***CRT Display Test Failures:*** If the CRT Display Test failed, troubleshoot as follows:

Step 1. Replace the CRT Monitor Assembly.

Step 2. Perform the CRT Monitor Test again; if fail, replace the A15, Graphics Processor PCB.

Step 3. Perform the CRT Monitor Test again; if fail, contact ANRITSU Customer Service Center.

***Front Panel Test Failures:*** If the Front Panel Test failed, troubleshoot as follows:

Step 1. Replace the Front Panel Assembly.

Step 2. Perform the Front Panel Test again; if fail, replace the A14, I/O#1 PCB.

Step 3. Perform the Front Panel Test again; if fail, contact ANRITSU Customer Service Center.

***External Keyboard Interface Test Failures:*** If the External Keyboard Interface Test failed, troubleshoot as follows:

Step 1. Replace the A18, Rear Panel PCB.

Step 2. Perform the External Keyboard Interface Test again; if fail, replace the A13, I/O#1 PCB.

Step 3. Perform the External Keyboard Interface Test again; if fail, contact ANRITSU Customer Service Center.

***Printer Interface Test Failures:*** If the Printer Interface Test failed, troubleshoot as follows:

Step 1. Replace the A18, Rear Panel PCB.

Step 2. Perform the Printer Interface Test again; if fail, replace the A13, I/O#1 PCB.

Step 3. Perform the Printer Interface Test again; if fail, contact ANRITSU Customer Service Center.

***GPIB Interface Test Failures:*** If the GPIB Interface Test failed, troubleshoot as follows:

Step 1. Replace the A18, Rear Panel PCB.

Step 2. Perform the GPIB Interface Test again; if fail, replace the A13, I/O#1 PCB.

Step 3. Perform the GPIB Interface Test again; if fail, contact ANRITSU Customer Service Center.

## 5-9 MEASUREMENT IN QUESTION

If the 373XXA measurement quality is suspect, the following paragraphs provide guidelines and hints for determining possible measurement quality problems.

The quality of 373XXA VNA measurements is determined by the following test conditions and variables:

- Condition of the 373XXA.
- Quality and condition of the interface connections and connectors.
- Quality and condition of the calibration components, through-lines, adapters and fixtures.
- Surrounding environmental conditions at the time of the measurement.
- Selection and performance of the calibration for the DUT being measured.

***Measurement Conditions Check List***

When determining possible measurement problems, check the following items:

1. Check the DUT and the calibration conditions:
   - ensure the Calibration Components Coefficients data has been installed into the system from the Calibration Kit in use.
   - ensure the proper calibration was done for the device being measured:
     - For high insertion loss device measurements the calibration should include isolation, high number of averages, and lower IF Bandwidth settings during the calibration.
     - For high return loss device measurements the calibration should also include a sliding load calibration.
   - Check DUT mating connector(s) condition and pin depth.
   - Measure an alternate known good DUT, if possible.
   - Check if the environment is stable enough for the accuracy required for the DUT measurement.
     - The system should not be subjected to variations in temperature.
     - The system should not be placed in direct sun light or next to a changing cooling source, such as a fan or air conditioning unit.
2. Check the calibration using known good components from the calibration kit. If measurements of these devices do not produce good results:
   - Check through-cable stability including condition and pin depth. Replace with a known good cable, if necessary.
   - Check condition and pin depth of calibration kit components. Replace with known good components, if necessary.
   - Check condition and pin depth of test port connectors. Replace with known good ones if necessary.

***NOTE***

The procedures for performing pin depth measurements for the connectors used on ANRITSU products are contained in Appendix C, Connector Maintenance Check Procedures.

3. Check the system performance as follows:
   - ❑ Perform the Signal Path Tests that are part of the Operational Tests. Refer to Chapter 3, Operational Tests.
   - ❑ Check Match, Directivity, and Dynamic Range as described in Chapter 4, Performance Verification.
   - ❑ Complete the remaining checks described in Chapter 4 (Performance Verification).

***Table 5-6.*** *Typical Reference Signal Values in dBm*

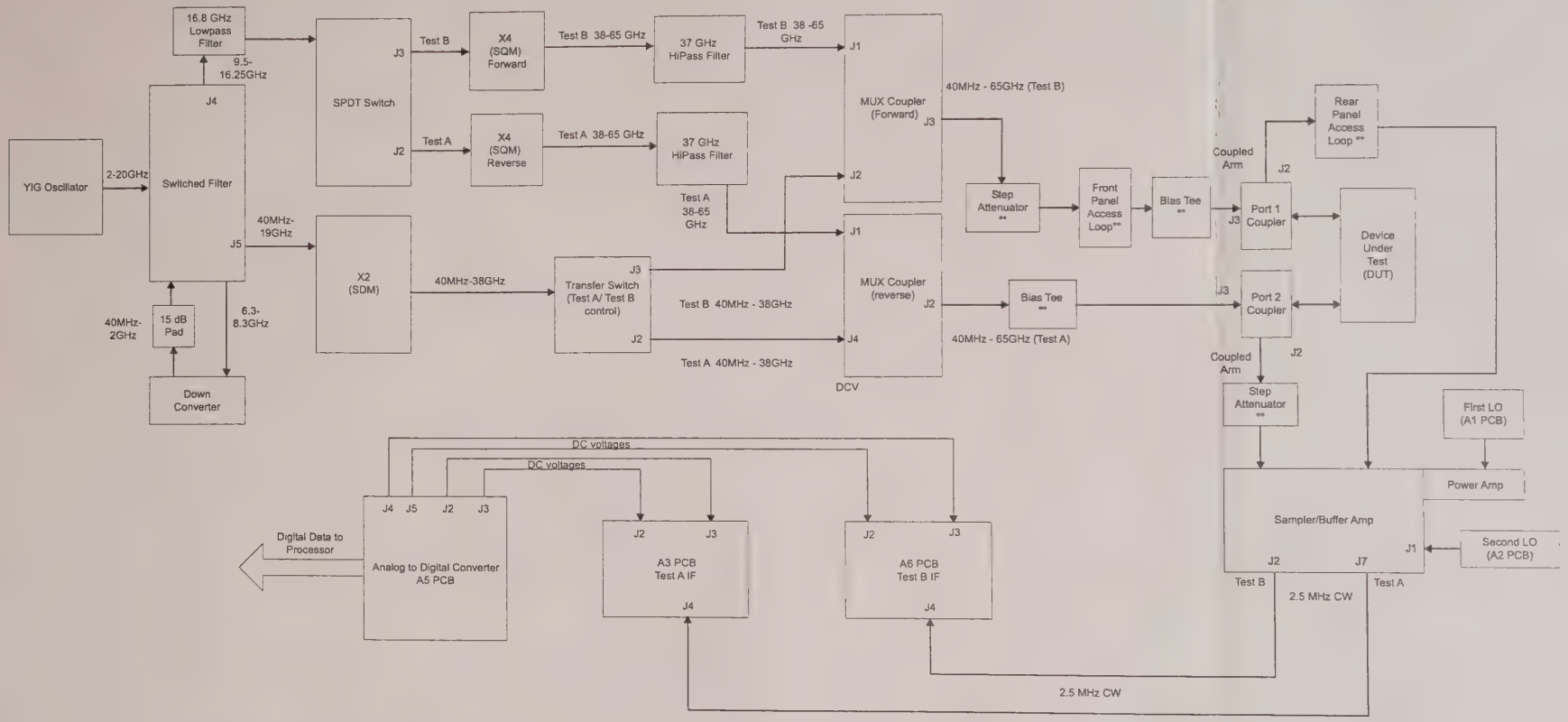
| Frequency | SQM In | SDM Out | MUX J4 | MUX J1 | Buffer Amp In |
|---|---|---|---|---|---|
| 20 GHz | NA | +18 | +6 | NA | –26 |
| 37 GHz | NA | +20 | +4 | NA | -28 |
| 40 GHz | +19 | NA | NA | +14 | -28 |
| 50 GHz | +18 | NA | NA | +14 | -23 |
| 65 GHz | +16 | NA | NA | +10 | -26 |

***Table 5-7.*** *Typical Transfer Switch Voltages (CW, Single Channel Display)*

| Wire Color | Below 38 GHz | | Above 38 GHz | |
|---|---|---|---|---|
| | S21 | S12 | S21 | S12 |
| Brown | +2.0 | –3.3 | +2.0 | +2.0 |
| Black | –6.7 | +1.6 | +1.6 | +1.6 |
| White | +1.6 | –6.8 | +1.6 | +1.6 |
| Grey | –3.3 | +2.0 | +2.0 | +2.0 |

***Figure 5-8.*** *Typical SPDT Switch Voltages (CW, Single Channel Display)*

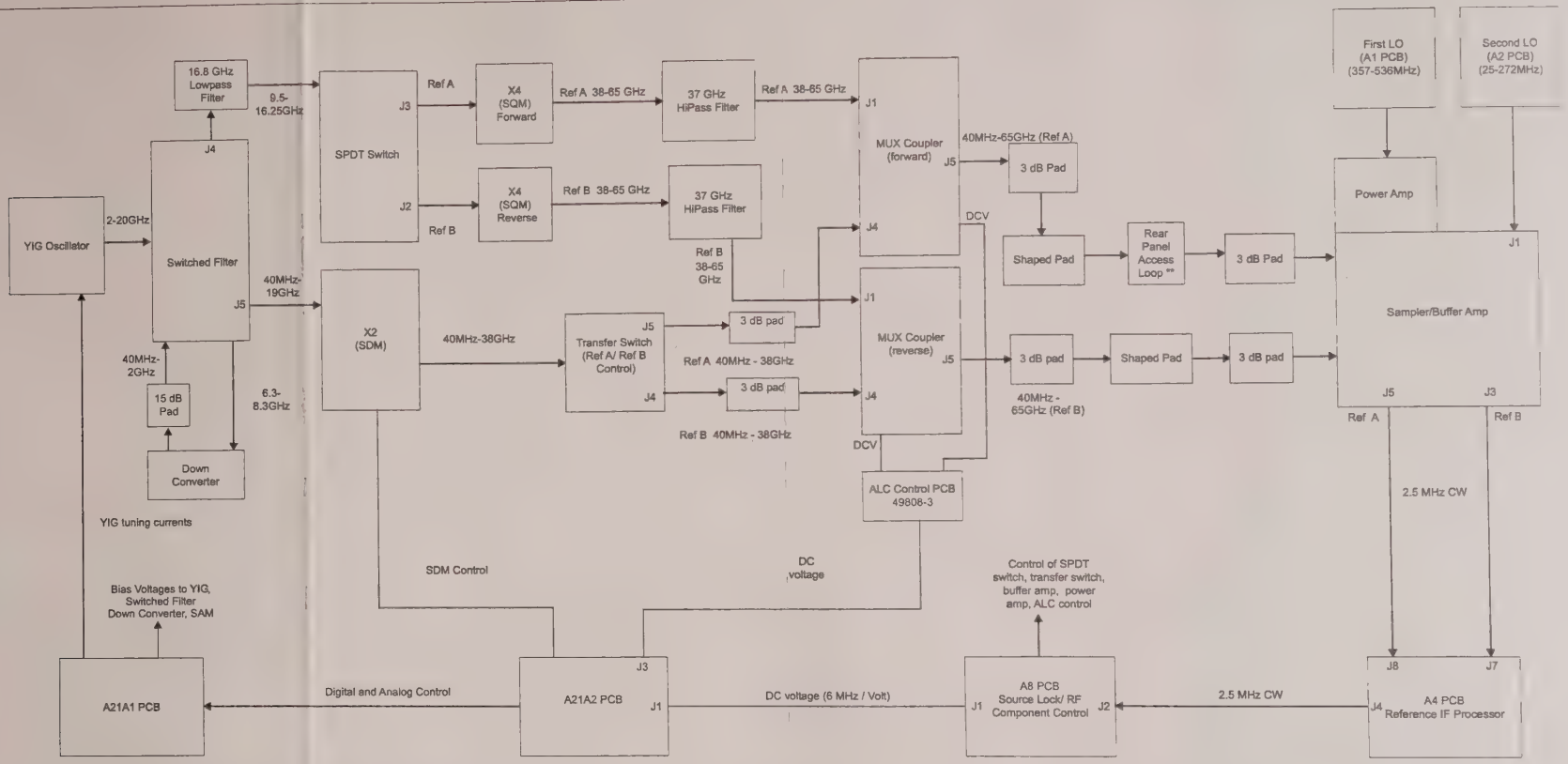
| Wire Color | Forward | Reverse |
|---|---|---|
| Brown | +1.2 | –3.7 |
| Grey | –3.7 | +1.2 |




NOTE: Sampler/Buffer amplifiers are individually matched to Power Amplifiers. If either fails, both should be replaced with another matched set, part number ND53249.

** Indicates not present on model 37297B or 37277B

**Figure 5-3.** *37397A Test Signal Path Diagram*




NOTE: Sampler/Buffer amplifiers are individually matched to Power Amplifiers. If either fails, both should be replaced with another matched set, part number ND53249.

** Indicates not present on model 37297B or 37277B

**Figure 5-4.** *37397A Source Lock Signal Path Diagram*

# *Chapter 6*
# *Adjustments*

## *Contents*


| | | |
|---|---|---|
| 6-1 | INTRODUCTION | 6-3 |
| 6-2 | LO1 CALIBRATION | 6-3 |
| | Calibration Procedure | 6-3 |
| | Post Calibration Actions | 6-3 |
| 6-3 | LO 2 CALIBRATION | 6-4 |
| | Calibration Procedure | 6-4 |
| | Post Calibration Actions | 6-5 |
| 6-4 | FREQUENCY CALIBRATION | 6-5 |
| | Calibration Procedure | 6-6 |
| | Post Calibration Actions | 6-7 |
| 6-5 | RF POWER/ALC CALIBRATION | 6-8 |
| | Calibration Procedure | 6-9 |
| | Post Calibration Actions | 6-10 |
| 6-6 | SOURCE LOCK THRESHOLD | 6-11 |
| | Calibration Procedure | 6-12 |
| | Post Calibration Actions | 6-12 |
| 6-7 | A8 ADJUSTMENT (37397A) | 6-13 |
| | Calibration Procedure | 6-13 |
| | Post Calibration Actions | 6-13 |
| 6-8 | A21A2 ADJUSTMENT (37397A) | 6-14 |
| | Calibration Procedure | 6-14 |
| | Post Calibration Actions | 6-15 |

# Chapter 6
# Adjustments

## 6-1 INTRODUCTION

This chapter contains procedures that are used to restore the calibration of the 373XXA signal source and the related source lock system assemblies. Use these procedures after various signal source related assemblies have been replaced due to troubleshooting or repair activities.

Please insure you have read and fully understand the servicing concepts for the 373XXA presented in Chapter 1 prior to continuing with this chapter.

## 6-2 LO1 CALIBRATION

This procedure uses the 373XXA internal diagnostics and calibration menus to adjust the A1 1st LO PCB assembly. Perform this calibation procedure if:

- The A1 PCB is replaced.
- BBRAM chip on A9 Processor PCB is replaced and the Source Lock Threshold Calibration data was not previously saved on disk (that is, data is not available for recall from a floppy disk).

***Calibration Procedure***

Perform the following steps:

***Equipment Required***

None

***NOTE***

Allow the 373XXA to warm-up at least 30 minutes prior to performing calibration.

***Procedure***

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS** then **LO1 CALIBRATION.**

Step 3. Follow the directions displayed on the 373XXA CRT screen, until calibration is completed.

***Post Calibration Actions***

After the calibration process is completed, perform the following actions, as appropriate:

***If calibration passes:***

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS |DISK OPERATIONS |SAVE TO HARD DISK|HW_CAL.LO1.**

***NOTE***

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type, date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

***If calibration fails:***

Step 1. Repeat the calibration. If it still fails, then proceed to Chapter 5, Troubleshooting.

## 6-3 LO 2 CALIBRATION

This procedure uses the 373XXA internal diagnostics and calibration menus to adjust the A2 2nd LO PCB assembly. Perform this calibation procedure if:

- The A2 PCB is replaced.
- BBRAM chip on A9 Processor PCB is replaced and the LO2 Calibration data was not previously saved on disk (that is, data is not available for recall from a floppy disk).

***Calibration Procedure***

Perform the following steps:

***Equipment Required***

None

***NOTE***

Allow the 373XXA to warm-up at least 30 minutes prior to performing calibration.

***Procedure***

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS** then **LO2 CALIBRATION.**

Step 3. Follow the directions displayed on the 373XXA CRT screen, until calibration is completed.

***Post Calibration Actions***

After the calibration process is completed, perform the following actions, as appropriate:

***If calibration passes:***

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.LO2.**

***NOTE***

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

***If calibration fails:***

Step 1. Repeat the calibration. If it still fails, then proceed to Chapter 5, Troubleshooting.

## 6-4 FREQUENCY CALIBRATION

This procedure uses the internal 373XXA diagnostics and calibration menus, in conjunction with a suitable frequency counter, to adjust the signal source frequencies throughout the range of the 373XXA model being calibrated. Perform this calibration procedure if:

- The Source FM/Lock Linearity test in Chapter 3, Operational Test, fails.
- Other testing or troubleshooting reveals a possible problem with the signal source frequency accuracy or phase lock loop.
- Any of the following assemblies are replaced:
  - A21A1 Source YIG/Bias
  - A21A2 Source Controller
  - Down Converter

- YIG Oscillator
- Switched Filter

- BBRAM chip on the A9 Processor PCB is replaced and the Source Calibration Data was not previously saved on disk (thus data could not be recalled from disk).

***Calibration Procedure***

Perform the following steps:

***Equipment Required***

Refer to Table 1-1, located on page 1-9, for further information about the following equipment:

EIP Model 578B Frequency Counter, or equivalent.

RF/Microwave Cable

GPIB cable, WILTRON 2100-2, or equivalent

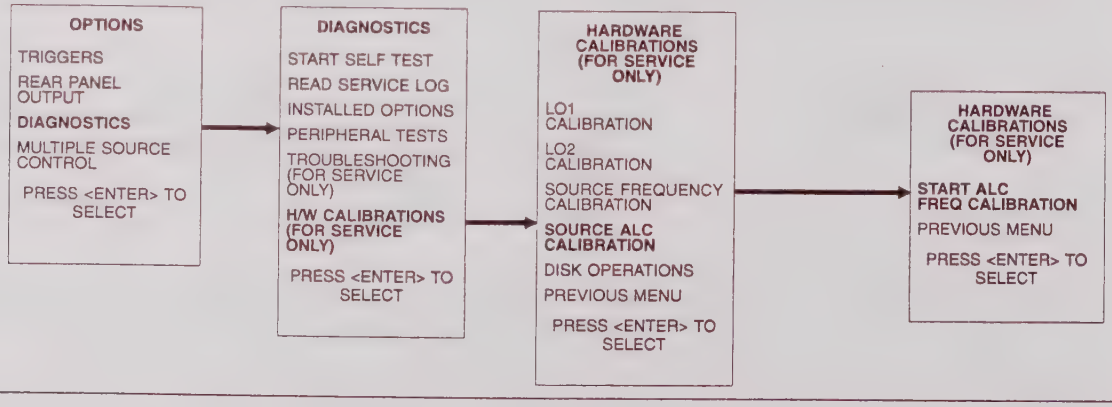
***NOTE***

Allow the 373XXA and Frequency Counter to warm-up at least 30 minutes prior to performing calibration.

***Procedure***

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu; then select in sequence: **H/W CALIBRATION**, and then **SOURCE FREQUENCY CALIBRATION** (below).



Step 3. Follow the directions displayed on the screen to set-up and connect the frequency counter to the 373XXA. Refer also to Figure 6-1 Select **START SOURCE FREQ CALIBRATION** from menu (above).

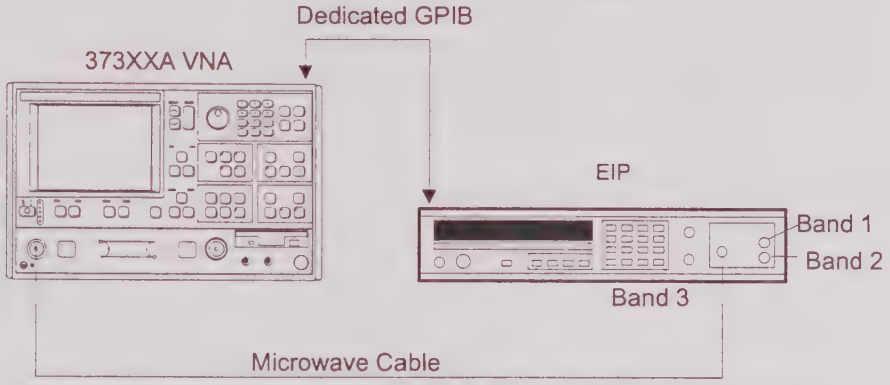



**Figure 6-1.** *Test Setup for Frequency Calibration*

Step 4. Follow the directions displayed on the 373XXA CRT screen, until calibration is completed.

***Post Calibration Actions*** After the calibration process is completed, perform the following actions, as appropriate:

***If calibration passes:***

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.FRE.**

***NOTE***

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type (FRE), date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

Perform the Source FM/Lock Linearity test in Chapter 3, Operational Tests. If the test fails, proceed to Chapter 5, Troubleshooting.

***If calibration fails:***

- Verify the GPIB cable is connected to the Dedicated GPIB (bottom) connector on the 373XXA rear panel.
- Verify that the frequency counter is functioning correctly, the cable is in good condition, and all connections are secure.
- Note which calibration step failed from the screen messages.
- Repeat the calibration. If it still fails, then go to Chapter 5, Troubleshooting.

## 6-5 RF POWER/ALC CALIBRATION

This procedure uses the 373XXA internal diagnostics and calibration menus, in conjunction with a suitable power meter, to adjust the output power level of the signal source throughout the range of the 373XXA model being calibrated. Perform this calibration procedure if:

- The Source Power/ALC test in Chapter 3, Operating Test, fails.
- Other testing or troubleshooting reveals a possible problem with RF Power accuracy or the ALC loop.
- Any of the following assemblies are replaced:
  - A21A1 Source YIG/Bias
  - A21A2 Source Controller
  - Down Converter
  - YIG Oscillator
  - Switched Filter
  - Transfer Switch
  - SDM (37369A)
  - Coupler (37325A and above)
  - Bridge (37317A and below)
  - Port 1 Source Step Attenuator
  - Buffer Amplifier
- BBRAM chip on the A9 Processor PCB is replaced and the Source Calibration Data was not previously saved on disk (thus data could not be recalled from disk).

***Calibration Procedure***

Perform the following steps:

***Equipment Required***

Refer to Table 1-1, located on page 1-9, for further information about the following equipment:

HP 437B Power Meter with HP 8487A Power Sensor

or:

ANRITSU ML24XXA with Version 2.02 or later, with ANRITSU Power Sensors MA2474A and SC6230 for 50 and 65 GHz units.

or:

Gigatronics 8541/8542 with 80304A Power Sensor

GPIB cable, WILTRON 2100-2, or equivalent

***NOTE***

Allow the 373XXA and power meter to warm-up at least 30 minutes prior to performing calibration.

***65 GHz Power Sensor Setup Procedure***

The Anritsu SC6230 Power Sensor has an internal frequency calibration factors table. The ML24XX meter settings must be changed so that the table will be used for frequencies above 50 GHz. To configure the meter for the new calibration factors table, proceed as follows:

Step 1. Press the Sensor key then **Cal Factor** softkey.

Step 2. Press the **More** softkey.

Step 3. Press the **Use Table** sofkey. Cursor will start blinking.

Step 4. Press 1 then the **Enter** softkey.

Step 5. Press the System key to exit.

***Procedure***

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu; then select in se-

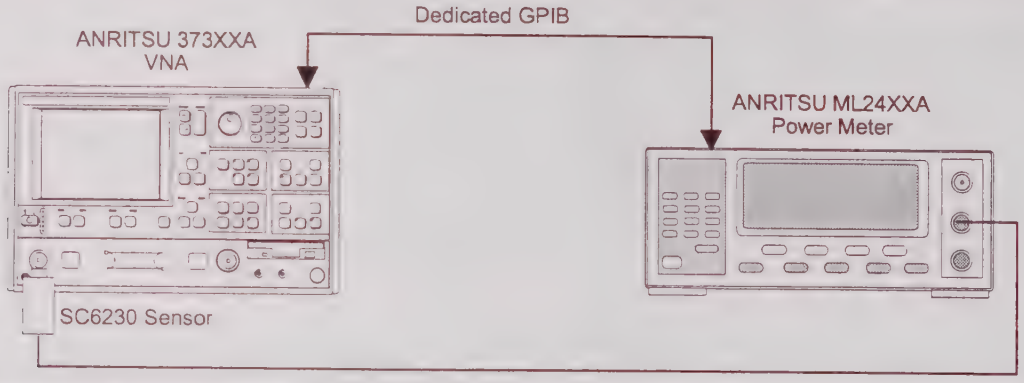
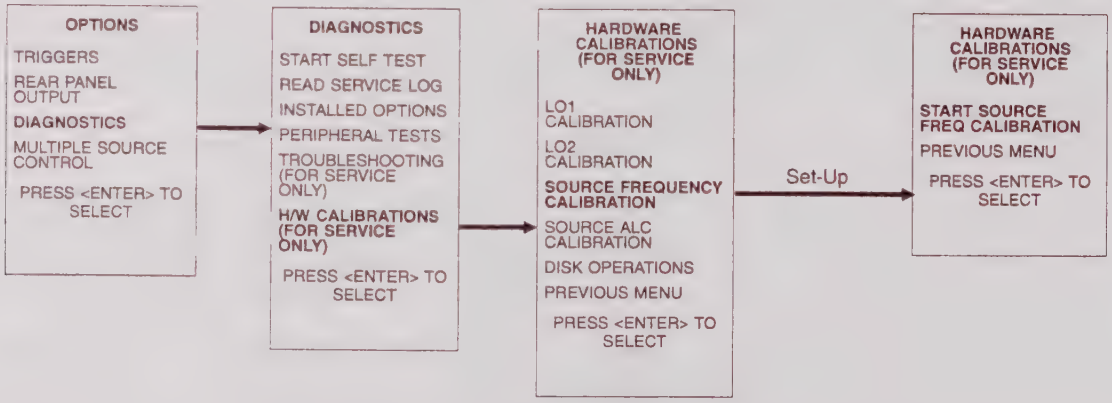



**Figure 6-2.** *Equipment Set-Up for RF Power / ALC Calibration*

quence: **H/W CALIBRATIONS, and then SOURCE ALC CALIBRATION** (below).




Step 3. Follow the directions displayed on the screen to set-up and connect the power meter to the 373XXA. Refer also to Figure 6-2. Select **START ALC CALIBRATION** from menu.

Step 4. Follow the directions displayed on the 373XXA CRT screen, until calibration is completed.

Step 5. If the software allows a Port 2 ALC Calibration, perform it now.

***Post Calibration Actions*** After the calibration process is completed, perform the following actions, as appropriate:

***If calibration passes:***

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.ALC.**

***NOTE***

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type (ALC), date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

Perform the RF Power Generation and Control test in Chapter 3, Operational Tests. If the test fails, proceed to Chapter 5, Troubleshooting.

**If calibration fails:**

- Verify the GPIB cable is connected to the Dedicated GPIB (bottom) connector on the 373XXA rear panel.
- Verify that the power meter and sensor are functioning correctly, the cables are in good condition, and all connections are secure.
- Verify the correct power sensor data exists in the power meter.
- Note the failed step in the calibration procedure from the screen messages.
- Repeat calibration. If it still fails then proceed to Chapter 5, Troubleshooting.

## 6-6 SOURCE LOCK THRESHOLD

This procedure uses the 373XXA internal diagnostics and calibration menus to adjust the source lock threshold of the phase-lock loop. Perform this calibation procedure if:

- The A4 PCB is replaced.
- BBRAM chip on A9 Processor PCB is replaced and the Source Lock Threshold Calibration data was not previously saved on disk (that is, data is not available for recall from a floppy disk).

***Calibration Procedure***

Perform the following steps:

***Equipment Required***

None

***NOTE***

Allow the 373XXA to warm-up at least 30 minutes prior to performing calibration, and perform the ALC calibration (paragraph 6-3) before doing this calibration.

***Procedure***

Step 1. If recalibrating a 37397A , install broadband terminations to both ports or install a throughline between ports.

Step 2. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 3. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS** then **SOURCE THRESHOLD CALIBRATION.**

Step 4. Follow the directions displayed on the 373XXA CRT screen, until calibration is completed.

***Post Calibration Actions***

After the calibration process is completed, perform the following actions, as appropriate:

***If calibration passes:***

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.SLT.**

***NOTE***

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type, date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

***If calibration fails:***

- Repeat the calibration. If it still fails, then proceed to Chapter 5, Troubleshooting.

## 6-7 A8 ADJUSTMENT (37397A)

The adjustments are important to the operation of the VNA above 56 GHz. Improperly adjusted A8 Potentiometers may cause lock failures. Perform these adjustments as follows:

- The A8 PCB is replaced.
- 44733 Buffer Amp is replaced.

### *Calibration Procedure*

Perform the following steps:

#### *Equipment Required*

None

***NOTE***

Allow the 373XXA to warm-up at least 30 minutes prior to performing calibration, and perform the ALC calibration (paragraph 6-3) before doing this calibration.

#### *Procedure*

Step 1. Connect a V Throughline (3670V50-2 with FF Adapter) between Ports 1 and 2.

Step 2. Set the 373XXA to sweep from 50 to 65 GHz.

Step 3. Set RF power to 0 dB (default value).

Step 4. Using Diagnostics menu, view Non-Ratio parameters.

Step 5. View Channel 1 (Ref A) only, and activate Autoscale.

Step 6. Adjust the "RA" potentiometer on top of A8 for the flattest trace display. A small discontinuity at 56 GHz is normal.

Step 7. Perform Step 6 for each of the four Non-Ratio channels.

### *Post Calibration Actions*

After the calibration process is completed, perform the following actions, as appropriate:

#### *If calibration passes:*

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.SLT.**

***NOTE***

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type, date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

***If calibration fails:***

- Repeat the calibration. If it still fails, then proceed to Chapter 5, Troubleshooting.

## 6-8 A21A2 ADJUSTMENT (37397A)

This adjustment ensures the correct RF power level will be available to drive the source quadrupler modules (SQMs). Perform these adjustments as follows:

- D454244 is replaced.
- A21A2 PCB is replaced.
- C21620 YIG Oscillator is replaced.

***NOTE***

Failure to perform this adjustment may result in intermittent operation.

***Calibration Procedure***

Perform the following steps:

Refer to Table 1-1, located on page 1-9, for further information about the following equipment:

HP 437B Power Meter with HP 8487A Power Sensor

or:

ANRITSU ML24XXA with Version 2.02 or later, with ANRITSU Power Sensors MA2474A and SC6230 for 50 and 65 GHz units.

or:

Gigatronics 8541/8542 with 80304A Power Sensor

GPIB cable, WILTRON 2100-2, or equivalent

***NOTE***

Allow the 373XXA and power meter to warm-up at least 30 minutes prior to performing calibration.

***Procedure***

Step 1. With power off and the new part installed, disconnect the RF cable from J4 of the Switched Filter.

Step 2. Install Power Sensor (use a 6 or 10 dB pad for protection) to Switched Filter J4.

Step 3. Turn on the 373XXA and set it to 38 GHz, CW.

Step 4. Adjust A21A2R238 for maximum power, but not over +26 dBm.

Step 5. Remove the pad and sensor and reconnect the RF cable to J4.

Step 6. Perform the procedures in paragraph 6-4 and 6-5 (frequency and ALC calibrations).

***Post Calibration Actions***

After the calibration process is completed, perform the following actions, as appropriate:

***If calibration passes:***

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.SLT.**

***NOTE***

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type, date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

***If calibration fails:***

Repeat the calibration. If it still fails, then proceed to Chapter 5, Troubleshooting.

# *Chapter 7*
# *System Description*

## *Table of Contents*


| | | |
|---|---|---|
| 7-1 | INTRODUCTION | 7-3 |
| 7-2 | SYSTEM OVERVIEW | 7-3 |
| 7-3 | ANALOG SUBSYSTEM ASSEMBLIES | 7-7 |
| | Signal Source Module | 7-7 |
| | Test Set Module | 7-8 |
| | A7 PCB, 10 MHz Timebase | 7-9 |
| | Receiver Module | 7-10 |
| | A8, Source Lock/ Signal Separation and Control PCB | 7-11 |
| | IF Section | 7-11 |
| | A7 PCB, LO3 | 7-12 |
| | A5 A/D Converter PCB | 7-12 |
| 7-4 | DIGITAL SUBSYSTEM ASSEMBLIES | 7-13 |
| | A9 Main Processor PCB Assembly | 7-13 |
| | A13 I/O Interface #1 PCB Assembly | 7-15 |
| | A14 I/O Interface #2 PCB Assembly | 7-15 |
| | A15 Graphics Processor PCB Assembly | 7-16 |
| | A16 Hard Disk PCB Assembly | 7-16 |
| | Floppy Disk Drive Assembly | 7-16 |
| | A24 VME Bus Terminator PCB | 7-16 |
| 7-5 | MAIN CHASSIS ASSEMBLIES | 7-16 |
| | A17 System Motherboard Assembly | 7-16 |
| | Front Panel Assembly | 7-16 |
| | Rear Panel Assembly | 7-17 |
| | A18 Rear Panel Interface PCB | 7-17 |
| | Power Supply Module | 7-18 |
| | Internal VGA Monitor | 7-19 |

# Chapter 7
# System Description

## 7-1 INTRODUCTION

This chapter provides a brief overview of the functional assemblies and major parts that comprise a typical Series 373XXA VNA system. It also briefly describes the operation of each major assembly.

## 7-2 SYSTEM OVERVIEW

Series 373XXA Vector Network Analyzers are ratio measurement systems used to measure complex vector signal characteristics (real/imaginary, magnitude/phase, etc) of devices and systems in the 22.5 MHz to 65 GHz frequency range.

The 373XXA performs these measurements by sourcing a stimulus signal to the Device Under Test (DUT) that is connected to the front panel Port 1 and/or Port2 connectors. (See Figure 7-1 on page 7-5). It simultaneously measures the DUT response, which consists of reflected and/or transmitted (attenuated, or amplified) signals at the connectors of the DUT. The reflected and/or transmitted signal(s) and a sample of the stimulus signal, are down converted and then transformed into their real and imaginary vector components. The resultant vector components are measured and converted into digital information. This digital information is sent to the Main Processor PCB where the desired S-parameter data is normalized and then presented to the user via the front panel color display. The display information is also sent to the rear panel VGA Out connector for use with an external VGA monitor.

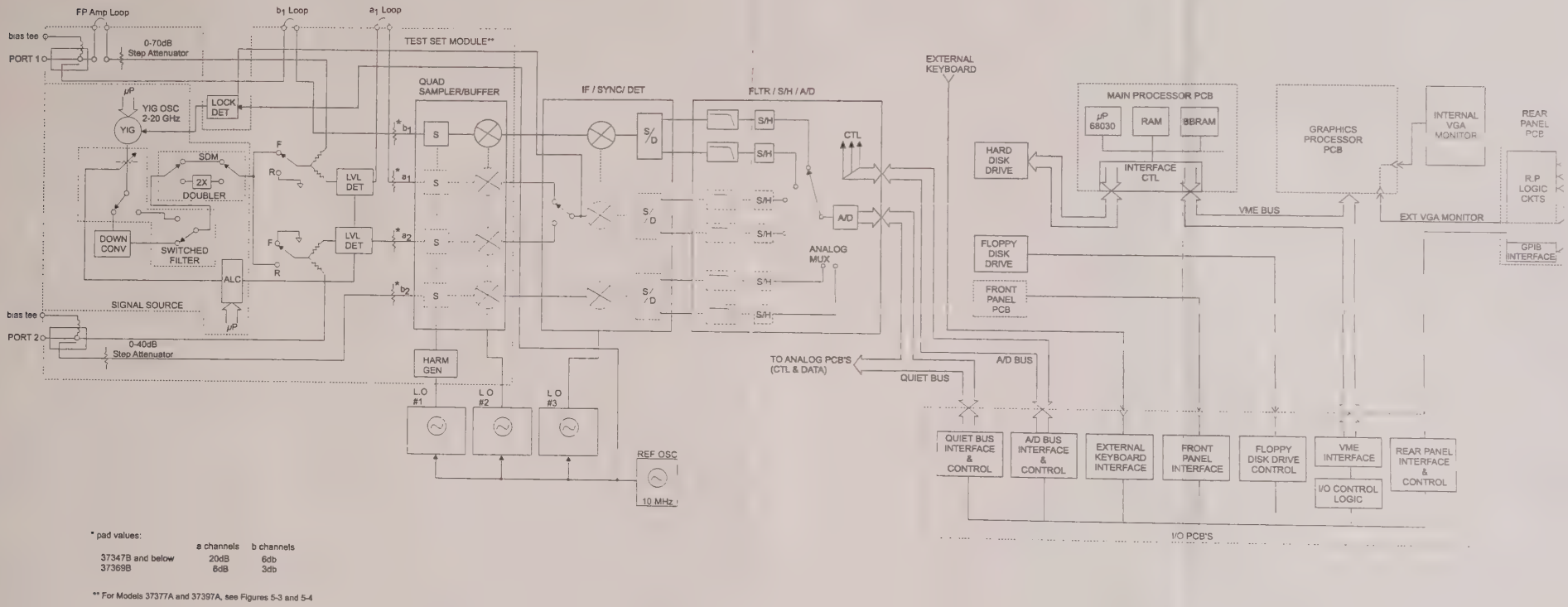
The normalized measurement information is also sent to the rear panel Printer Out connector for use with an external printer and/or plotter.

A front panel keypad, a rotary knob, and an IBM compatible keyboard interface provide user interaction with 373XXA Main Processor PCB.

The system is equipped with internal hard disk and floppy disk drives and battery backed internal memories for storage and retrieval of data and front panel setup information.

The 373XXA implements an IEEE 488.2 interface. This GPIB interface allows an externally connected instrument controller to control the 373XXA system in the "Remote-Only" mode. All 373XXA measurement and input/output operations may be controlled remotely in this mode.

An internal service log stores a record of system failures, data about the failures, and other key system service information. The service log is implemented using internal battery-backed SRAM memory.

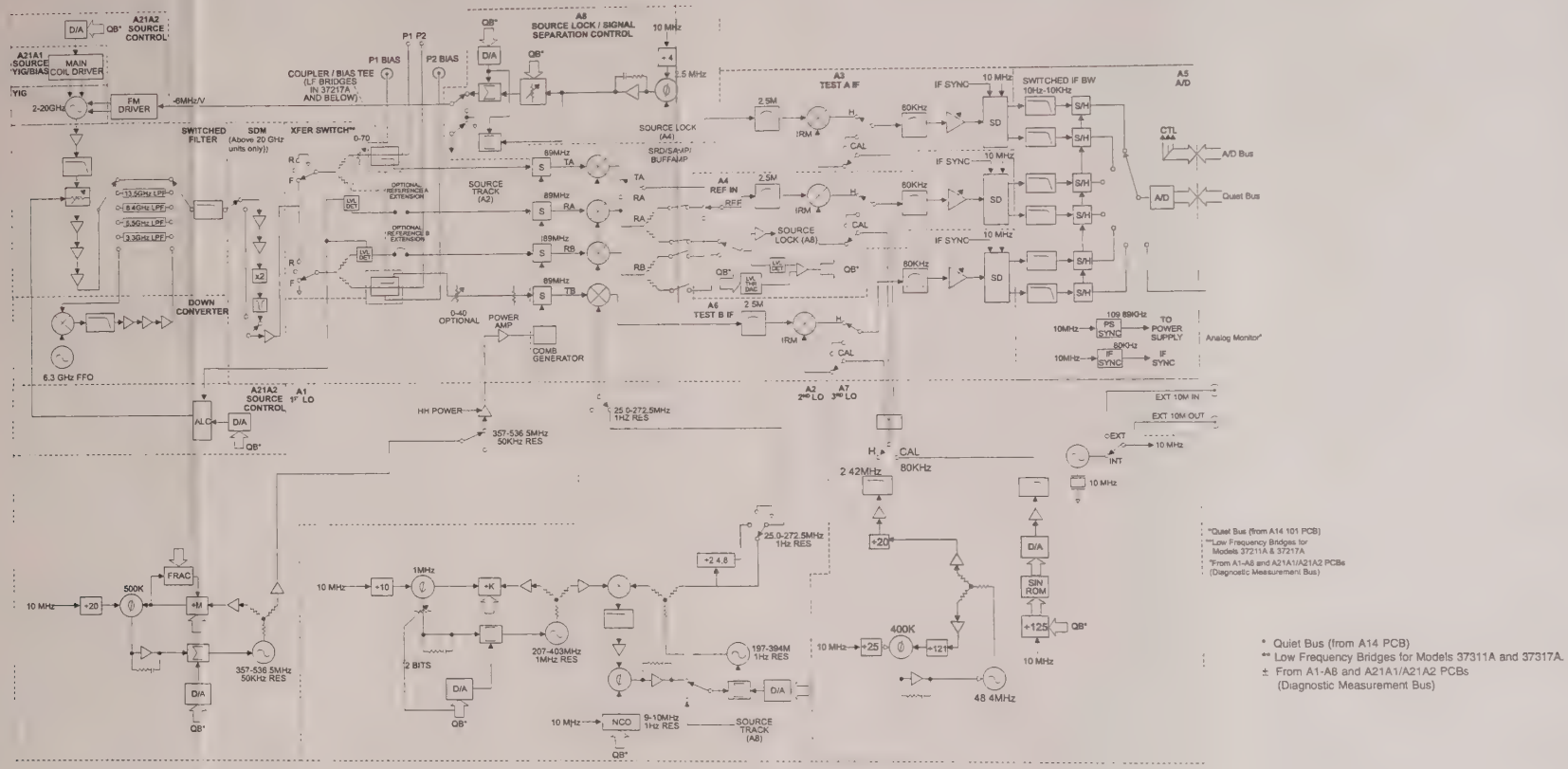



* pad values:

| | a channels | b channels |
|---|---|---|
| 37347B and below | 20dB | 6db |
| 37369B | 8dB | 3db |

** For Models 37377A and 37397A, see Figures 5-3 and 5-4

**Figure 7-1.** *Overall Block Digram of 373XXA VNA System*




* Quiet Bus (from A14 PCB)
** Low Frequency Bridges for Models 37311A and 37317A.
± From A1-A8 and A21A1/A21A2 PCBs (Diagnostic Measurement Bus)

** For Models 37377A and 37397A, see Figures 5-3 and 5-4

372XX17.CDR

**Figure 7-2.** *Analog Subsystem Block Diagram*

## 7-3 ANALOG SUBSYSTEM ASSEMBLIES

The following paragraphs briefly describe the major assemblies that comprise the 373XXA Analog Subsystem. Descriptions of the functions performed by each assembly are also included.

### *Signal Source Module*

The Signal Source Module consists of the items listed below; refer to the block diagram of the Analog Subsystem (Figure 7-2) at left.

- 2-20 GHz YIG Oscillator Assembly
- A21A1 YIG/Bias Controller PCB
- A21A2 Source Control PCB
- Switched Filter Assembly
- Down Converter Assembly

The Signal Source Module is a swept frequency signal generator that produces a phase locked (and leveled) output signal within a range of 22.5 MHz to 20 GHz. All Series 373XXA VNA models employ phase-lock control of the signal source module so that the output frequency is accurate and stable. The output signal is phase locked by the –6 MHz/volt control signal fed back from the A8 Source Lock/Separation Control PCB Assembly (which is described in following paragraphs).

All Series 372XXB VNA models use a single YIG-tuned oscillator to produce fundamental frequency source signals from 2.0 to 20 GHz. All other output frequencies are derived from the fundamental frequencies generated by the YIG-tuned oscillator. The signal source output frequencies for the low end portion of the frequency range (22.5 MHz to 2.0 GHz) are produced by down converting YIG fundamental signals in the range of 6.3225 to 8.3 GHz.

For Model 37369A, the signal source output frequencies for the high end portion of the frequency range (20 to 40 GHz) are produced by the Switched Doubler Module that doubles the YIG fundamental signals in the range of 10 to 20 GHz. The Switched Doubler Module (SDM) is located in the Test Set Module (described below.) The A21A2 Source Control PCB assembly provides all bias and control signals for the SDM.

The YIG-tuned oscillator generates a high-power RF output signal that has low broadband noise and low spurious content. The frequency of the YIG-tuned oscillator is controlled by means of :

- The YIG main tuning coil
- The YIG FM (fine tuning) coil

The system A9 Main Microprocessor PCB sends the data that represents the desired operating frequency to the A21A2 (Source Control) PCB, which converts the frequency data to analog signals. These sig-

nals are then sent to the A21A1 YIG/Bias Controller PCB. This PCB converts the analog signals to YIG main tuning coil current.

The main tuning coil current from A21A1 YIG/Bias Controller PCB coarsely tunes the YIG-tuned Oscillator to within a few megahertz of the final output frequency. The YIG phase-lock loop then fine tunes the YIG-tuned oscillator to the exact output frequency via the FM (fine tuning) coil.

The fundamental frequency source signal is leveled by a PIN Diode attenuator that is part of the Switched Filter Assembly. This attenuator is controlled by the Automatic Leveling Control (ALC) circuits that are located on the A21A2 Source Control PCB. The input to the ALC circuits is the DC feed-back signal from the leveling detectors located in the Test Set Module.

Depending on the frequency of operation, the fundamental signal is passed through one of four low-pass filters located in the Switched Filter Assembly. The cut-off frequencies for these filters are 3.3 GHz, 5.5 GHz, 8.4 GHz, and 13.5 GHz, respectively. The signal is then passed through a 20 GHz high pass filter before being routed either directly to the Test Set Module, or to the Down-Converter Assembly .

The signal is switched to the Down-Converter Assembly only when the 373XXA is operating in the low end portion of its frequency range. The frequency of the output signal from the Down-Converter Assembly is 22.5 MHz to 2 GHz for Models 37311Aand 37317A and 40 MHz to 2 GHz for Models 37225B and above. The output signal from the Down-Converter Assembly is routed to the Test Set Module.

***Test Set Module***

The Test Set Module consists of the items listed below; refer to Figure 7-2.

- Transfer Switch assembly
- Two Couplers (Models 37325A and above) or two Low Frequency Bridges (Models 37317A and below)
- Switched Doubler Module for 20-40 GHz operation (Model 37369A)

In the Test Set Module, the 22.5 MHz – 20 GHz signal from the signal source module is switched (via the Transfer Switch) between the front panel Port 1 and Port 2 connectors. The Transfer Switch is controlled by the A9 Main Processor PCB to set the direction of signal flow for the desired test (Port 1 = Forward; Port 2 = reverse). For operation between 20 GHz and 40 GHz, the stimulus signal is routed to the Switched Doubler Module before being sent to the Transfer Switch.

The stimulus signal is output to the DUT via directional couplers mounted directly to the Port 1 and Port 2 front panel connectors. Note that bridges are used instead of couplers in RF Models 37211B and 37217B.

Each output circuit path from the Transfer Switch contains a splitter. One path from each splitter goes to the associated directional coupler (Port 1/Port 2) and the other path feeds the associated "Reference" input of the Receiver Module (RA/RB), via a level detector. The output generated by the two parallel configured level detectors is a DC signal that corresponds to the output level of the stimulus signal. This signal is the input signal for the ALC circuits located in the signal source module. Only the detector in the currently selected sweep direction actually generates the ALC control signal.

The Test Set simultaneously receives the reflected and transmitted device-under-test (DUT) signals via the Port 1/Port 2 directional couplers. These two test signals, along with a sample of the output RF stimulus (Reference) signal, are sent to the Receiver Module.

The a1 Reference signal is routed out of, and back into, the 373XXA via extension loop located on the rear panel. This allows for injection of user supplied signals in lieu of internal signals.

***A7 PCB, 10 MHz Timebase***

Except for units equipped with Option 10 or 10A, the A7 PCB contains the 10 MHz TCXO Reference Timebase that is the master timebase for the system. It also contains the signal distribution and switching functions for all External/Internal 10 MHz reference signals.

The A7 PCB provides the fixed 2.42 MHz Local Oscillator signal and the 80 kHz Calibration signal to the IF PCBS (A3, A4, and A6). These signals are derived from the 10 MHz Reference Timebase.

Units equipped with Option 10 or 10A have a high-stability ovenized timebase mounted inside the rear panel directly above the Power Supply Module. This timebase replaces the standard 10 MHz timebase located on the A7 PCB. The output from this timebase is routed to the A7 PCB for distribution. It is powered by regulated +24 vdc from the A7 PCB.

### *Receiver Module*

The Receiver Module consists of the items listed below; refer to Figure 7-2.

- Quad Sampler/Buffer Amplifier with integrated SRD (step recovery diode)
- Power Amplifier
- A1, LO1 PCB
- A2, LO2 PCB

The Receiver Module is a four channel two stage Sampler/Buffer Amplifier and Down Conversion unit. It simultaneously converts the four 22.5 MHz - 40 GHz signals from the Test Set Module into three 2.5 MHz IF signals that are output to the IF Section.

The first stage of the Receiver Module uses harmonic sampling to down-convert the four 22.5 MHz – 40 GHz output signals from the Test Set Module down to 89 MHz signals. Any input signals below 270 MHz are passed directly through the four harmonic samplers to the second stage without down-conversion. The drive signal to each of the harmonic samplers is a comb of harmonics generated by a step recovery diode (SRD).

The Power Amplifier provides the signal that drives the SRD. The input to the Power Amplifier is the 357 – 536.5 MHz signal from the A1 First Local Oscillator (LO1) PCB. Regardless of the operating frequency, the Power Amplifier is biased on at all times to insure optimum thermal stability.

The second stage of the Receiver Module uses the 25.0 – 272.5 MHz signal from the A2 Second Local Oscillator (LO2) PCB to down-convert the 89 MHz signals into four 2.5 MHz IF signals TA, TB, RA, RB (two test signals and two reference signals). Either the Reference A or the Reference B IF signal is selected, as is appropriate for Forward/Reverse operation. The resultant three 2.5 MHz IF signals (Test A, Test B, and Reference A/B) are output to the IF Section. A buffered version of the Reference A/B signal is also fed to the A8 Source Lock/Signal Separation Control PCB as the Source Lock signal.

The Receiver Module can also select the Reference A IF signal that is output to the IF Section via the Test A switch path. This IF signal is used during Line Reflect Line (LRL) Calibrations to ratio the Reference A and Reference B signals.

***A8, Source Lock/ Signal Separation and Control PCB***

The Source Lock Phase Comparator circuit on the A8 Source Lock/ Signal Separation Control PCB compares the Source Lock (Reference A/B) signal from the Receiver Module with a signal derived from the10 MHz reference oscillator. The output of this circuit is the –6 MHz/V correction signal, which is routed to the circuit on the A21A2 Source Control PCB that generates the FM coil tuning current signal. This signal is output to the A21A1 YIG/Bias Controller PCB to fine tune the YIG-tuned oscillator to the exact output frequency. When the YIG-tuned oscillator outputs the exact frequency, the two inputs to the phase comparator circuit on the A8 PCB match and the phase-lock loop is locked.

The A8 PCB Assembly also provides bias and control signals to the Test Set and Receiver Modules for operating the following circuits:

- Transfer Switch
- Power Amplifier
- Quad/Sampler Buffer Amplifier
- Front Panel Forward/Reverse LEDs

***IF Section***

The IF Section consists of the items listed below; refer to Figure 7-2.

- A3 Test A IF PCB
- A4, Reference IF PCB
- A5, A/D Converter PCB
- A6, Test B IF PCB
- A7, Third Local Oscillator, LO3, PCB

The IF Section converts the three 2.5 MHz IF signals from the Receiver Module into six DC output signals. The A3 (Test A), A4 (Reference A/B), and A6 (Test B) PCBs down-convert the 2.5 MHz input IF signals to 80 kHz IF signals and then adjust their amplitude for input to the synchronous detector stage of each PCB. Each 80 kHz IF signal is synchronously detected and converted into a pair of DC signals that contain the information for the real and imaginary portions of the original 80 KHz IF signal. Thus, the three IF signals (two test signals and the reference signal) yield six DC signals that fully represent the real and imaginary vector components of the DUT's S-parameters.

The IF Section also checks the 2.5 MHz phase lock signal for proper power level by comparing it to a known reference level on the A4 PCB. A sample of the 2.5 MHz Reference A/B IF signal is sent to the A8 Source Lock/Separation Control PCB assembly for phase locking the signal source module. The A3 and A6 PCBs are functionally identical and physically interchangeable.

***A7 PCB, LO3***

The A7, Third Local Oscillator (LO3) Assembly, provides a fixed 2.42 MHz Local Oscillator signal that is used on the A3, A4, and A6 PCBs to down-convert the 2.5 MHz IF signals to 80 kHz. It also provides an 80 kHz standard signal for the IF Section Calibration process that occurs automatically approximately every six minutes. This automatic IF Section Calibration is one of the 373XXA features that ensures rated measurement accuracy. Automatic IF Calibration can be turned off and/or invoked at any time during measurement sweeps.

***A5 A/D Converter PCB***

The A5 A/D Converter PCB contains a six-channel, two stage, switched-filter sample-and-hold circuit and a 20 bit A/D converter. Each of the six DC signals from the A3, A4, and A6 PCBs are input to a separate channel of the PCB. The first stage of each channel is a low-pass filter with four selectable cutoff frequencies of 10 kHz, 1 kHz, 100 Hz, and 10 Hz. The second stage of each channel is a sample-and-hold amplifier that stores the signals during the A/D conversion process. Each channel is sequentially selected for input to the 20 bit A/D converter.

The A5 A/D Converter PCB also derives the 109.89 kHz Power Supply Synchronization Signal and the 80 kHz IF Synchronization Signal from the 10 MHz Reference Timebase. Additional functions of the A5, A/D Converter Assembly include:

- Measurement of power supply voltages and other internal nodes of the 372XXB for diagnostic purposes.
- Measurement of an externally applied analog input signal. This function is used for service purposes only.
- External Trigger Input signal processing (from rear panel)
- External Analog Output signal generation (to rear panel)

The A/D converter circuitry located on the A/5 PCB is used as a DVM to measure various internal system analog monitor points on the A1 – A8 and A21A1/ A21A2 PCBs. It is also used to monitor power supply voltages and other critical points throughout the 373XXA, which can be readout via the Diagnostics Menus. DVM readings are also recorded in the service log for certain system failures.

## 7-4 DIGITAL SUBSYSTEM ASSEMBLIES

The following paragraphs briefly describe the major assemblies that comprise the 373XXA Digital Subsystem. The digital subsystem provides all system control, I/O interface, digital signal processing, and data presentation functions.

The major assemblies that comprise the 373XXA digital PCB subsystem are listed below. Refer to Figure 7-3, at left.

- A9, Main Processor PCB
- A13, I/O Interface #1 PCB
- A14, I/O Interface #2 PCB
- A15, Graphics Processor PCB
- A16, Hard Disk PCB
- A18, Rear Panel Interface
- Rear Panel Assembly
- Front Panel Assembly
- Floppy Disk Assembly
- A24, VME Bus Terminator PCB

### *A9 Main Processor PCB Assembly*

The major components that comprise the A9 Main Processor PCB are:

- 68040 Microprocessor (w/ integrated co-processor) – This is the CPU for the 372XXB system.
- 4 MB DRAM – This is the main system memory. This memory is volatile (non-battery backed). During normal operation, it stores the 372XXB software that is loaded from disk at power-up.
- 8 KB BBRAM – This auxiliary memory chip contains a back-up battery that is continuously recharged whenever power is applied. (The back-up battery has a four year minimum life span.) This chip also contains real time and date clock functions. It is used to store low level boot-up parameters, ALC calibration data, source frequency calibration data, and service log header data.
- 512 KB SRAM – This auxiliary memory is backed-up by a non-rechargeable Lithium battery that provides 200 days (maximum) of power-off protection. It is used to store current and saved front panel setups, trace/normalization data, current RF calibration data, current sweep frequency data, flat power calibration data, and the service log error list.
- VME Bus interface chip – This chip is used to interface the Main Processor PCB to the A13, A14, and A15 digital PCBs (via the VME bus interface).
- SCSI Bus interface – This chip is used to interface the Main Processor PCB to the A16 Hard Disk PCB.

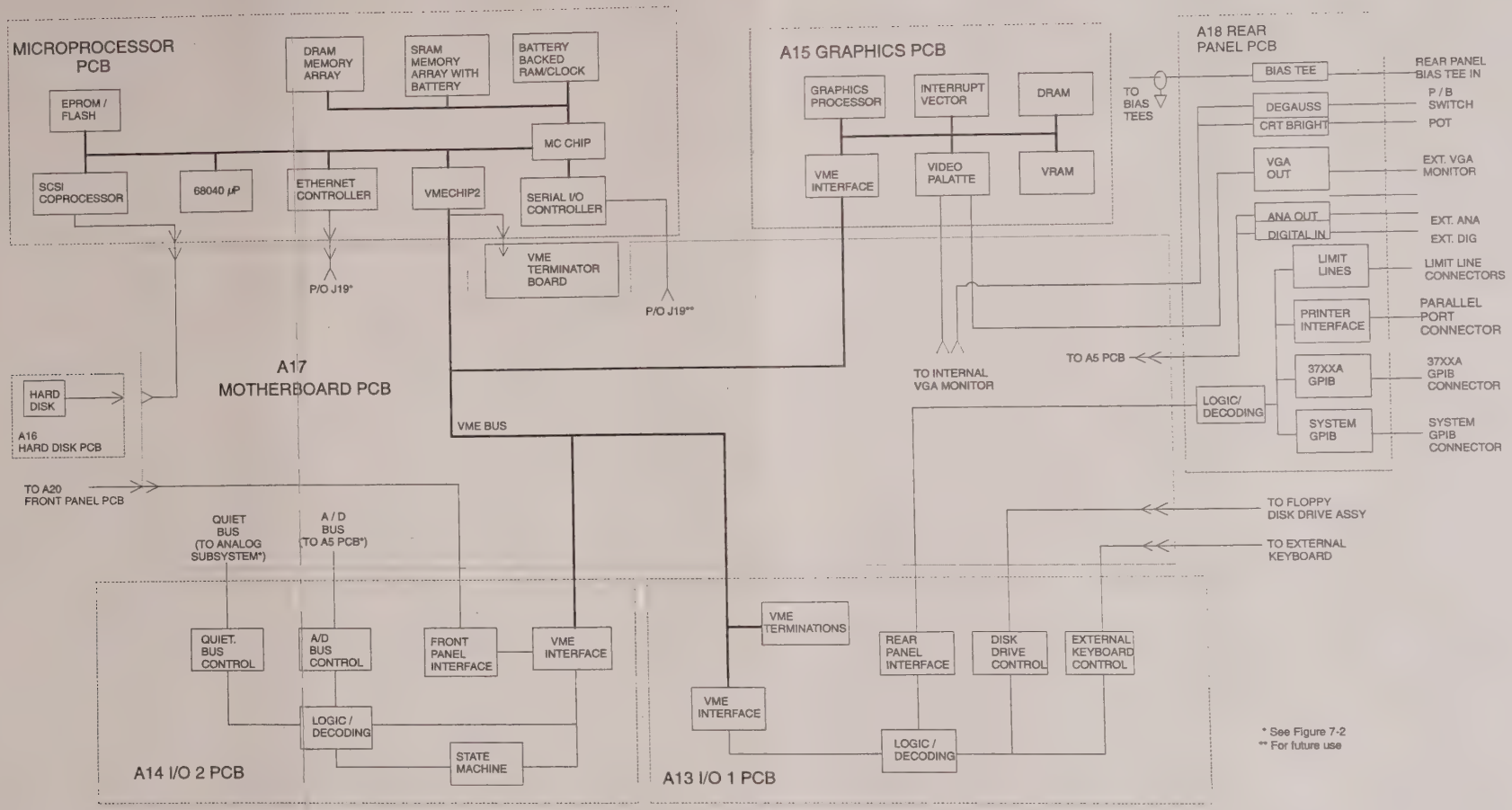



**Figure 7-3.** *DigitalSubsystem Block Diagram*

## 7-4 DIGITAL SUBSYSTEM ASSEMBLIES

The following paragraphs briefly describe the major assemblies that comprise the 373XXA Digital Subsystem. The digital subsystem provides all system control, I/O interface, digital signal processing, and data presentation functions.

The major assemblies that comprise the 373XXA digital PCB subsystem are listed below. Refer to Figure 7-3, at left.

- A9, Main Processor PCB
- A13, I/O Interface #1 PCB
- A14, I/O Interface #2 PCB
- A15, Graphics Processor PCB
- A16, Hard Disk PCB
- A18, Rear Panel Interface
- Rear Panel Assembly
- Front Panel Assembly
- Floppy Disk Assembly
- A24, VME Bus Terminator PCB

### *A9 Main Processor PCB Assembly*

The major components that comprise the A9 Main Processor PCB are:

- 68040 Microprocessor (w/ integrated co-processor) – This is the CPU for the 372XXB system.
- 4 MB DRAM – This is the main system memory. This memory is volatile (non-battery backed). During normal operation, it stores the 372XXB software that is loaded from disk at power-up.
- 8 KB BBRAM – This auxiliary memory chip contains a back-up battery that is continuously recharged whenever power is applied. (The back-up battery has a four year minimum life span.) This chip also contains real time and date clock functions. It is used to store low level boot-up parameters, ALC calibration data, source frequency calibration data, and service log header data.
- 512 KB SRAM – This auxiliary memory is backed-up by a non-rechargeable Lithium battery that provides 200 days (maximum) of power-off protection. It is used to store current and saved front panel setups, trace/normalization data, current RF calibration data, current sweep frequency data, flat power calibration data, and the service log error list.
- VME Bus interface chip – This chip is used to interface the Main Processor PCB to the A13, A14, and A15 digital PCBs (via the VME bus interface).
- SCSI Bus interface – This chip is used to interface the Main Processor PCB to the A16 Hard Disk PCB.

- System boot-up EPROM – This chip contains the boot-up instructions used by the system CPU at power-up.

***A13 I/O Interface #1 PCB Assembly***

This PCB assembly performs the following functions:

- Floppy drive control – interface for the Floppy Drive Assembly.
- External Keyboard control – interface for the front panel Keyboard connector.
- Interface for the A18 Rear Panel PCB Assembly (below).
- Interface and control for the rear panel IEEE 488.2 GPIB and Dedicated GPIB interface connectors.

***A14 I/O Interface #2 PCB Assembly***

This PCB assembly contains a State Machine controller, decode logic, and bus interface control circuits that perform the following functions:

- Quiet Bus interface control. The Quiet Bus passes control and data signals from the A9 Main Processor PCB to the A1 – A8, and A21 PCBs and returns status and data signals back to the A9 PCB. This bus is managed by the control circuits on the A14 PCB such that it is inactive during the the time that a measurement is being taken.

  ***NOTE***

  The output data from the A5 PCB A/D converter is sent to the A9 Main Processor PCB via the Quiet Bus, the A14 PCB, and the VME Bus.

- A/D Bus interface control. During the measurement process, all A/D selection and conversion functions on the A5 PCB are controlled exclusively by the A14 PCB State Machine Controller. This is accomplished via the command lines of the A/D Bus.
- Measurement control functions – the A14 PCB State Machine Controller manages many of the 373XXA functions during a measurement, as follows:
  - Quiet Bus interface control
  - A/D Bus interface control:
    - Sample and Hold control for A5 PCB
    - A/D selection and conversion control for A5 PCB
  - Check for phase lock condition
  - Gain ranging
  - Delay generation for IF Bandwidth setting function

The A14 PCB also provides the interface to the Front Panel A19 and A20 PCBs

***A15 Graphics Processor PCB Assembly***

This PCB assembly contains circuitry that simultaneously drives both the internal VGA monitor and an external VGA monitor (if used), as follows:

- It receives measurement and display information from the A9 Main Processor PCB and generates screen display (video) information.
- Provides interface and control for the internal VGA Monitor Assembly.
- Provides interface for an external monitor via the rear panel VGA Out connector.

***A16 Hard Disk PCB Assembly***

The PCB assembly contains a pre-formatted hard disk drive assembly and associated interface circuitry. The A16 PCB interfaces directly with the A9 Main Processor PCB via the (A9) SCSI interface.

***Floppy Disk Drive Assembly***

This unit is a standard 1.44 MByte DOS compatible format floppy disk drive. It is physically mounted to the test set tray (not to the Front Panel Assembly). It interfaces to the system via the A13 I/O Interface #1 PCB.

***A24 VME Bus Terminator PCB***

This PCB assembly terminates the VME bus to insure stable digital data transfer on the bus. It plugs into the VME bus structure on the bottom surface of the A17 Motherboard Assembly.

## 7-5 MAIN CHASSIS ASSEMBLIES

The assemblies described below are the major assemblies mounted to the basic frame of the 373XXA.

***A17 System Motherboard Assembly***

The motherboard assembly provides signal routing and D.C. power distribution paths for all major PCB assemblies of the Analog Subsystem (A1 – A8) and the Digital Subsystem (A9 – A16). It also contains the VME Bus, Quiet Bus, and A/D Bus structures and other signal routing paths. It does not contain any active components.

***NOTE***

The motherboard assembly is an integral part of the 373XXA chassis. It is not a field replaceable unit.

***Front Panel Assembly***

The Front Panel Assembly consists of the following assemblies and parts:

- A19 Front Panel Switch PCB – this assembly contains all of the front panel switches for the 373XXA VNA.
- A20 Front Panel Control PCB – this assembly contains the decode logic for the switches located on the A19 Front Panel Switch PCB. This PCB interfaces with the A14 I/O Interface #2 PCB Assembly.
- Front Panel LEDs, beeper, keys, controls, and connectors
- Front panel overlay

- Front panel casting

***NOTE***

The front panel is an integrated assembly that is replaceable only as a single unit.

***Rear Panel Assembly***

The Rear Panel Assembly includes the following rear panel connectors:

- 10 MHz Reference In and Out BNC connectors
- External Trigger BNC connector
- External Analog Input BNC connector
- External Analog Output BNC connector

This assembly also includes:

- Reference Channel Extension Loops (Option 11)
- Main system fan
- The A18 Rear Panel PCB and associated connectors, circuitry, and cables (below).

***A18 Rear Panel Interface PCB***

This PCB assembly contains the rear panel connectors listed below. It also includes the associated circuitry and cabling interfaces that link these connectors (and the rear panel fan assembly) to the A17 Motherboard PCB and other assemblies within the 373XXA.

- IEEE 488.2 GPIB connector (with associated interface circuits)
- Dedicated GPIB connector (with associated interface circuits)
- Printer Out connector (with associated interface circuits)
- VGA Out connector
- CRT degauss and brightness controls
- I/O Connector (and associated interface circuits)– This 25 pin miniature D-sub connector contains:
  - Limits Testing Status TTL outputs
  - Port 1 and Port 2 Bias Inputs.
  - Ext Dig In signal (same as External Trigger BNC)
  - Ext Ana Out signal (same as External Analog Output BNC)

The A18 PCB also contains:

- Routing of –24 Vdc power to the rear panel system fan.
- Routing of External Analog Out and External Trigger Input signals to the Mother Board.

### *Power Supply Module*

The Power Supply Module is a single self contained assembly mounted on the rear panel. This module provides:

- Unregulated +5, +9, ±18, and ±27 Vdc supply voltages to the other assemblies of the 372XXB.
- Dedicated AC line connection for the Internal VGA Monitor.
- Thermal and over-current shutdown protection circuitry
- Sensing and input power regulation for operation with 85 – 264 VAC, 48 – 63 Hz, universal AC line input power.
- Internal fan cooling (for power supply module)
- Supply voltages distribution

Table 7-1 identifies all 372XXB DC power supply voltages and lists their usage by the various PCB assemblies. Unless otherwise indicated, supply voltages are regulated on the assembly using them. The analog and digital power supply grounds are isolated.

***NOTE***

All power supply voltages listed in Table 7-1 can be accessed via the A/D bus for measurement by the the A/D converter circuitry (e.g., DVM) located on the A5 A/D PCB assembly.

***Table 7-1.*** *372XXB Power Supply Voltages and Usages*

| Voltage | Assemblies Where Used |
|---|---|
| +5V | A1, A2, A3, A4, A5, A6, A7, A9, A13, A14, A15, A16, A18, A19/A20 (P.O. Front Panel), A21A1/A21A2 (P.O. Source Module), A24, External Keyboard |
| +9V | A1, A2, A7, A8 |
| +18V | A1, A2, A3, A4, A5, A6, A7, A8, A13 |
| -18V | A1, A2, A3, A4, A5, A6, A7, A8, A13 |
| +27V | A1, A2, A5, A7 |
| -27V | A5, A18 |
| The following supply voltages are derived from the +/-18 supply voltages on the A13 I/O #1 PCB: | |
| +12V | A9, A15 |

### *Internal VGA Monitor*

The internal monitor assembly is powered from a dedicated AC Line from the Power Supply Module. The degaussing and brightness controls for the internal monitor are located on the rear panel for easy access by the operator. There are no internal adjustments for this unit.

***NOTE***

The internal monitor assembly is not a field repairable unit.

# *Chapter 8*
# *Remove and Replace Procedures*

## *Table of Contents*


| | | |
|---|---|---|
| 8-1 | INTRODUCTION | 8-3 |
| 8-2 | EQUIPMENT REQUIRED | 8-3 |
| 8-3 | COVERS | 8-4 |
| 8-4 | A1–A9 AND A13–A16 PCBS | 8-6 |
| | A1 – A9 PCBs | 8-6 |
| | A13 – A16 PCB's | 8-6 |
| 8-5 | A9 PCB BBRAM CHIP | 8-6 |
| 8-6 | A9 PCB SRAM BATTERY | 8-10 |
| 8-7 | A24 VME BUS TERMINATOR PCB | 8-12 |
| 8-8 | FRONT PANEL ASSEMBLY | 8-12 |
| 8-9 | VGA DISPLAY MONITOR | 8-14 |
| 8-10 | LIQUID CRYSTAL DISPLAY (LCD) | 8-16 |
| 8-11 | FLOPPY DISK DRIVE | 8-17 |
| 8-12 | REAR PANEL ASSEMBLY | 8-19 |
| 8-13 | FAN ASSEMBLY | 8-21 |
| 8-14 | POWER SUPPLY MODULE | 8-21 |
| 8-15 | A18 REAR PANEL PCB | 8-22 |
| 8-16 | TEST SET MODULE ASSEMBLIES | 8-25 |
| | Transfer Switch | 8-25 |
| | Input Coupler(s)/ Low Freq Bridge(s) | 8-26 |
| | Power Amplifier | 8-26 |
| | Buffer Amplifier/ Sampler(A31) | 8-27 |
| | Switched Doubler Module Assembly | 8-28 |

8-17 SIGNAL SOURCE MODULES . . . . . 8-29
Removal of Signal Source Module . . . . . 8-29
A21A2 Source Control PCB . . . . . 8-31
A21A1 Source YIG Bias Control PCB . . . . . 8-32
Switched Filter Assembly . . . . . 8-33
Down Converter Assembly . . . . . 8-33
YIG Oscillator Assembly . . . . . 8-34

8-16 REMOVE / REPLACE TEST SET MODULE ASSEMBLIES . . . . . 8-25
Transfer Switch . . . . . 8-25
Input Coupler(s)/Low Freq Bridge(s) . . . . . 8-26
Power Amplifier . . . . . 8-26
Buffer Amplifier/Sampler(A31) . . . . . 8-27
Switched Doubler Module Assembly . . . . . 8-28

8-17 REMOVE / REPLACE SIGNAL SOURCE MODULE ASSEMBLIES . . . . . 8-29
Removal of Signal Source Module . . . . . 8-29
A21A2 Source Control PCB . . . . . 8-31
A21A1 Source YIG Bias Control PCB . . . . . 8-32
Switched Filter Assembly . . . . . 8-33
Down Converter Assembly . . . . . 8-33
YIG Oscillator Assembly . . . . . 8-34

# Chapter 8
# Remove and Replace Procedures

## 8-1 INTRODUCTION

This chapter provides procedures for removing and replacing 373XXA field exchangeable assemblies and components. When using these procedures, please observe the warning and caution notices below.

***WARNING***

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels.

***CAUTION***

Many assemblies in the 373XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

## 8-2 EQUIPMENT REQUIRED

All procedures in this chapter require the use of either a #1 or #2 size Phillips type screw driver. Any additional tool requirements are specified at the beginning of each procedure.

## 8-3 COVERS

Adjustment and troubleshooting operations require removal of the top cover. Replacement of some 373XXA assemblies and parts require removal of all covers. The following procedures describe this process.

***NOTE***

It is only necessary to loosen the 373XXA handle assemblies to remove the top, bottom, or side covers. However, if the front panel is to be removed, remove the handle assemblies at this time.

***Preliminary:***

❑ Switch the 373XXA power **off**. Remove the power cord.

***Procedure:***

Step 1. Loosen (or remove) the right and left handle assemblies, as follows:

- Place the 373XXA on its top (bottom-side up).
- Loosen/remove the screws at the sides of the handle assemblies.
- If removing handles, pull them away from unit and set aside.

***CAUTION***

The green headed screws have Metric threads.

Step 2. To remove the top cover:

- Place the 373XXA in normal (top-side up) position.
- Remove the feet from the two top corners at the rear of the 373XXAB (Figure 7-1).
- Remove the center screw from rear of the top cover.
- Lift and slide the top cover away from the 373XXA.

Step 3. To remove the bottom cover:

- Place the 373XXA on its top (bottom-side up).
- Remove the feet from the two bottom corners at the rear of the 373XXA.
- Remove the center screw from rear of the bottom cover.
- Lift and slide the top cover away from the 373XXA.

Step 4. To remove the left cover:

- Place the 373XXA on its right side (monitor down).
- If not already done, remove the feet from the two left-side corners at the rear of the 373XXA.
- Remove two center screws from the left cover.
- Remove the center screw from rear of the left side cover.
- Lift and slide the side cover away from the 373XXA.

Step 5. To remove the right cover:

- Place the 373XXA its left side (monitor up).
- If not already done, remove the feet from the two right-side corners at the rear of the 373XXA.
- Remove the center screw from rear of the right side cover.
- Remove the center screw from rear of the right side cover.
- Lift and slide the side cover away from the 373XXA.

To replace the instrument covers, perform the steps above in the reverse order.

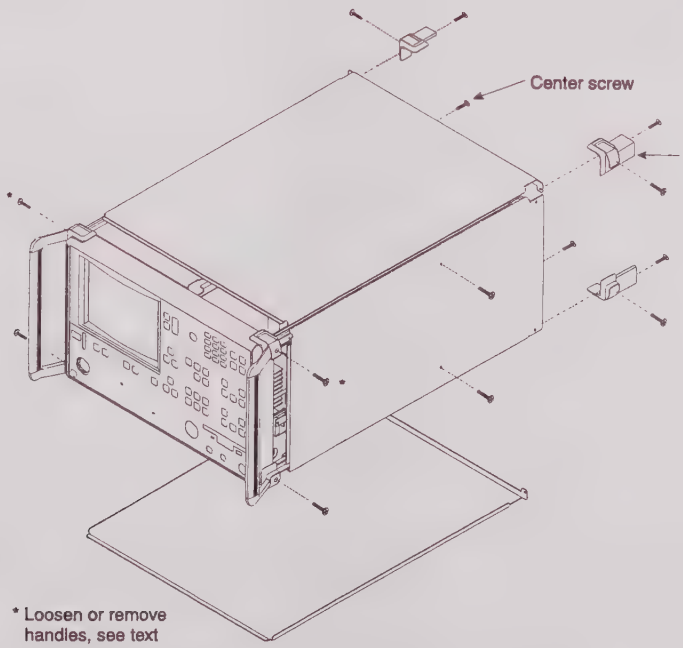



**Figure 8-1.** *Exploded View of 372XXB Chassis Covers*

## 8-4 A1–A9 AND A13–A16 PCBS

This paragraph provides instructions for removing and replacing the A1– A9 and A13 – A16 PCB's, which are located underneath the covers of the large and small card-cages, respectively.

***Preliminary:***

❑ Switch the 373XXA power **off**. Remove the power cord.

Remove the top cover (paragraph 8-3).

### *A1 – A9 PCBs*

***Procedure:***

Step 1. Place the 373XXA in normal (top-side up) position.

Step 2. Remove the two screws that secure the large card-cage cover (Figure 8-2).

Step 3. Remove the large card-cage cover and set aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight up.

To replace the PCB(s) and covers, perform the steps above in the reverse order.

### *A13 – A16 PCB's*

***Procedure:***

Step 1. Place the 373XXA in normal (top-side up) position.

Step 2. Remove the two screws that secure the large card-cage cover (Figure 8-2).

Step 3. Remove the large card-cage cover, then remove the small card-cage cover and set aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight up.

To replace the PCB(s) and covers, perform the steps above in the reverse order.

## 8-5 A9 PCB BBRAM CHIP

This paragraph provides instructions for removing and replacing the BBRAM Chip located on the A9 Main Processor PCB assembly.

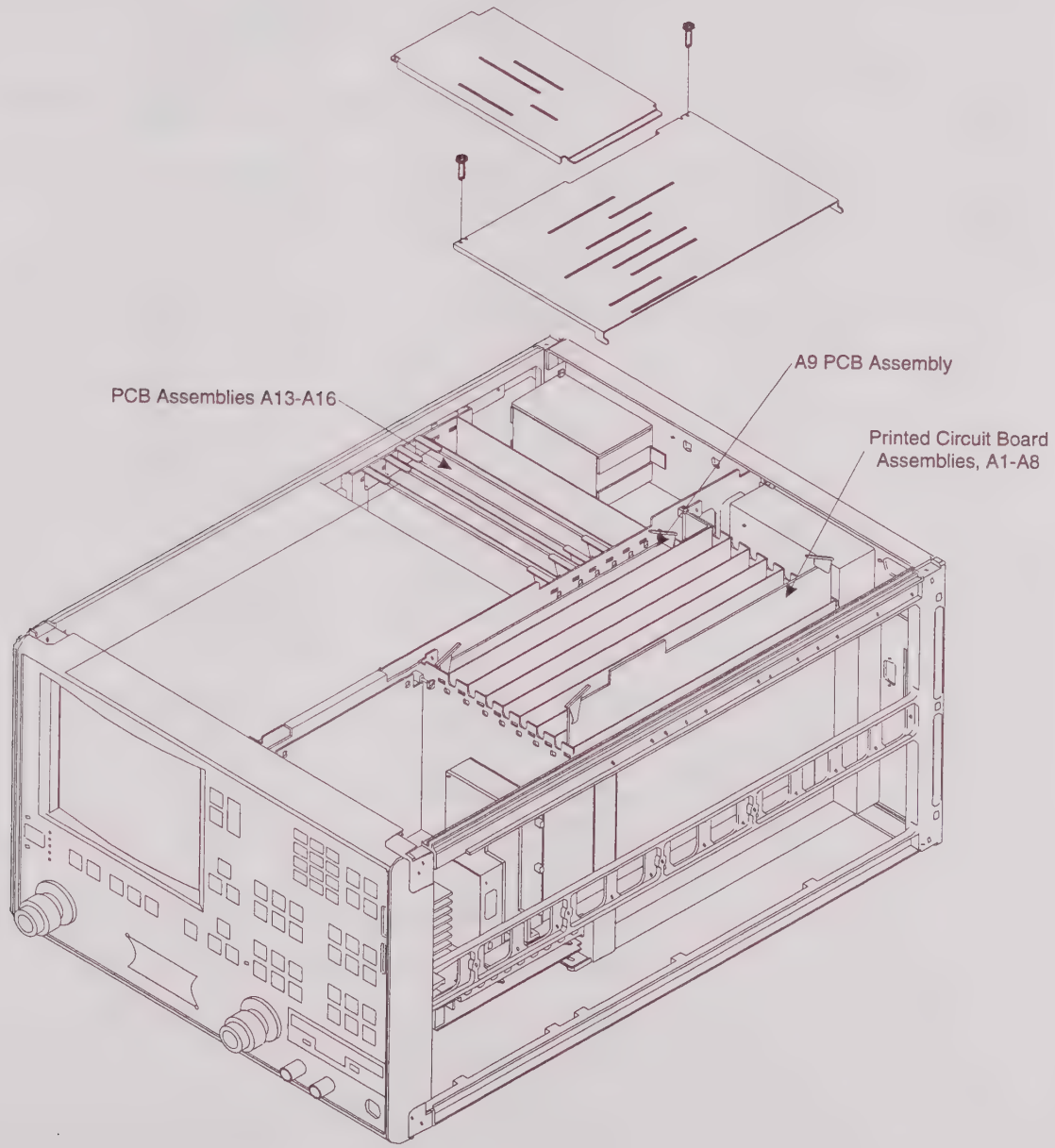
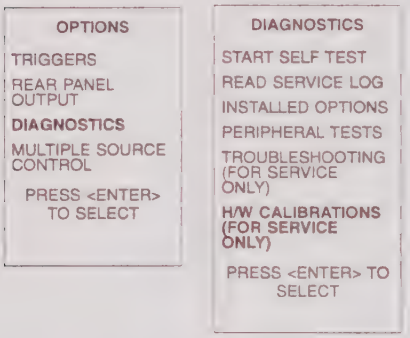



**Figure 8-2.** *A1-A9 and A13-A16 PCB Assemblies Removal Diagram*

*Preliminary:*

Before removing and replacing the BBRAM Chip it is necessary to save the following calibration data to the hard disk: signal source Frequency, ALC, Source Lock Threshold, LO1 and LO2. Proceed as follows:

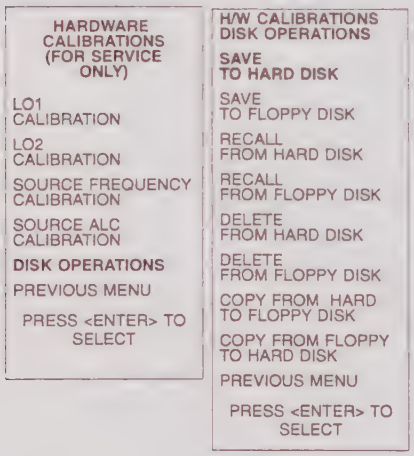



Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu (left).

Step 2. Select **DIAGNOSTICS** from the menu. Then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.ALL.**

***NOTE***

Also save the calibration data to floppy disk. Label the disk with calibration type (ALL), date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.




Step 3. Switch the 373XXA power **off**. Remove the power cord.

***Remove/Replace Procedure:***

Step 1. Remove the top cover and the large card-cage cover to expose the A1 – A9 PCBs (refer to paragraph 8-4).

Step 2. Remove the A9 PCB from the unit.

Step 3. Locate and remove the BBRAM chip from the A9 PCB. See Figure 8-3.

Step 4. Replace the BBRAM chip on the A9 PCB.

Step 5. Reinstall the A9 PCB, the large card-cage cover, and the top cover.

Step 6. Reconnect power cord. Switch 373XXA power **on**.

***Post Replacement Procedure:***

Recall the calibration data saved in the Preliminary step from the floppy disk as follows:

Step 1. Insert the floppy disk with the previously saved Source Frequency and ALC Calibrations Data in the 373XXA floppy disk drive.

Step 2. Select DIAGNOSTICS from the menu (left). Then select in sequence: H/W CALIBRATIONS | DISK OPERATIONS | RECALL CAL FROM FLOPPY DISK | HW_CAL.ALL.

OPTIONS
TRIGGERS
REAR PANEL OUTPUT
**DIAGNOSTICS**
MULTIPLE SOURCE CONTROL
PRESS <ENTER> TO SELECT

**DIAGNOSTICS**
START SELF TEST
READ SERVICE LOG
INSTALLED OPTIONS
PERIPHERAL TESTS
TROUBLESHOOTING (FOR SERVICE ONLY)
**H/W CALIBRATIONS (FOR SERVICE ONLY)**
PRESS <ENTER> TO SELECT

**HARDWARE CALIBRATIONS (FOR SERVICE ONLY)**
LO1 CALIBRATION
LO2 CALIBRATION
SOURCE FREQUENCY CALIBRATION
SOURCE ALC CALIBRATION
**DISK OPERATIONS**
PREVIOUS MENU
PRESS <ENTER> TO SELECT

**H/W CALIBRATIONS DISK OPERATIONS**
SAVE TO HARD DISK
SAVE TO FLOPPY DISK
RECALL FROM HARD DISK
**RECALL FROM FLOPPY DISK**
DELETE FROM HARD DISK
DELETE FROM FLOPPY DISK
COPY FROM HARD TO FLOPPY DISK
COPY FROM FLOPPY TO HARD DISK
PREVIOUS MENU
PRESS <ENTER> TO SELECT

***NOTE***

If unable to recall calibrations from disk, you must redo the calibration data described in the Preliminary step on the preceeding page.

Step 3. Ensure the system sweeps several times without errors.

Step 4. Refer to Chapter 3, Operational Tests. Perform the following:

- Check the Service Log for any new errors. (Note that the service log is non-volatile; it may contain error entries from a previous problem or service operation.)
- Run the Self Test procedure.
- Refer to Chapter 5, Troubleshooting, if any system errors are reported.

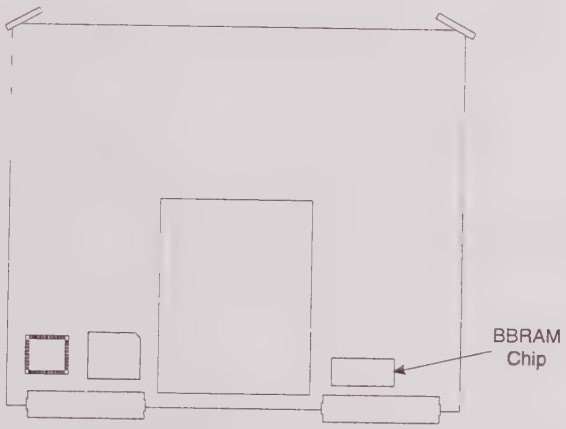



**Figure 8-3.** *Location of BBRAM Chip on the A9 PCB*

## 8-6 A9 PCB SRAM BATTERY

This paragraph provides instructions for removing and replacing the SRAM Battery located on the A9 Main Processor PCB assembly.

***Preliminary:***

❑ Switch the 373XXA power **off**. Remove the power cord.

***CAUTION***

The SRAM battery incorporates flammable materials such as lithium and organic solvents. If lithium batteries, such as this one, are mistreated or incorrectly handled, they may *burst open and ignite*. This can result in possible injury or fire. When handling the SRAM battery, carefully following the following precautions:

- DO NOT short circuit.
- DO NOT disassemble, deform, or apply excessive pressure.
- DO NOT heat or incinerate.
- DO NOT apply solder directly.
- DO NOT mix model or new and old batteries.
- DO NOT charge.
- ALWAYS check that proper polarity is observed.

***Remove/Replace Procedure:***

Step 1. Remove the top cover and the large card-cage cover to expose the A1 – A9 PCBs (refer to paragraph 8-4).

Step 2. Remove the A9 PCB from the unit.

Step 3. Locate and carefully remove the SRAM battery from the A9 PCB. See Figure 8-4.

Step 4. Replace the SRAM battery on the A9 PCB, as follows:
- Insure that the pins are clean.
- Note the polarity and carefully press the batterly into the socket.

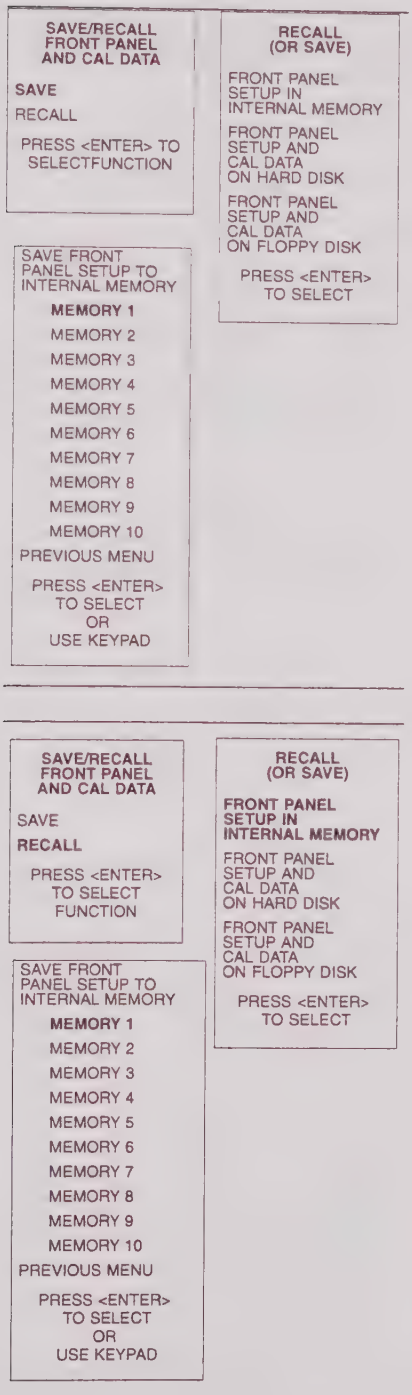
Step 5. Reinstall the A9 PCB, the large card-cage cover, and the top cover.

***Post Replacement Procedure:***

Step 1. Connect power cord. Switch 373XXA power **on**.

Step 2. Ensure the system sweeps several times without errors.

Step 3. Refer to Chapter 3, Operational Tests. Perform the following:




- Check the Service Log for any new errors. (Note that the service log is non-volatile; it may contain error entries from a previous problem or service operation.)
- Run the Self Test procedure.
- Refer to Chapter 5, Troubleshooting, if any system errors are reported.

Step 4. Use front panel keys to set to Dual Channel Display 1 & 3.

Step 5. Save front panel setup to memory as follows:

- Press the Save/Recall Menu key
- Select SAVE from menu (top left): then in sequence select: FRONT PANEL SETUP IN INTERNAL MEMORY | MEMORY 1

Step 6. Reset system to default settings by pressing the Default key.

Step 7. Ensure the system resets to back to the default Quad-Channel display. Refer to Chapter 5, Troubleshooting, if it does not.

Step 8. Recall the saved memory 1 setup as follows:

- Press the Save/Recall Menu key
- Select RECALL from menu (bottom left): then in sequence select: FRONT PANEL SETUP IN INTERNAL MEMORY | MEMORY 1

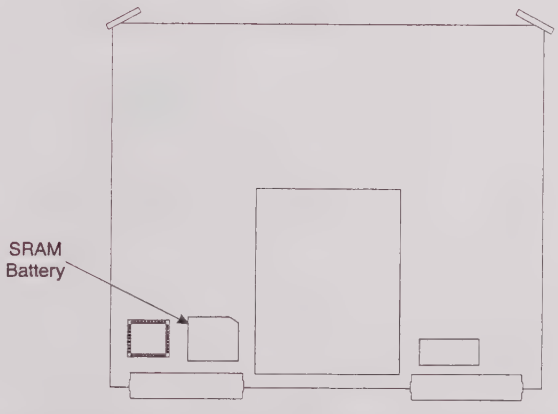



**Figure 8-4.** *Location of SRAM Battery on the A9 PCB*

## 8-7 A24 VME BUS TERMINATOR PCB

This paragraph provides instructions for removing and replacing the A24 VME Bus Terminator PCB assembly.

***Preliminary:***

- ❑ Switch 373XXA power **off**. Remove the power cord.
- ❑ Remove bottom cover (paragraph 8-3).

***Remove/Replace Procedure***

Step 1. Place the 373XXA on its top (bottom-side up).

Step 2. Locate the A24 PCB assembly (Figure 8-5). Unplug A24 PCB assembly from the A17 Motherboard PCB by gently pulling straight up on each side.

***CAUTION***

Be careful not bend or disturb the hard co-ax lines located near right edge of A24 PCB.

## 8-8 FRONT PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the 373XXA Front Panel assembly.

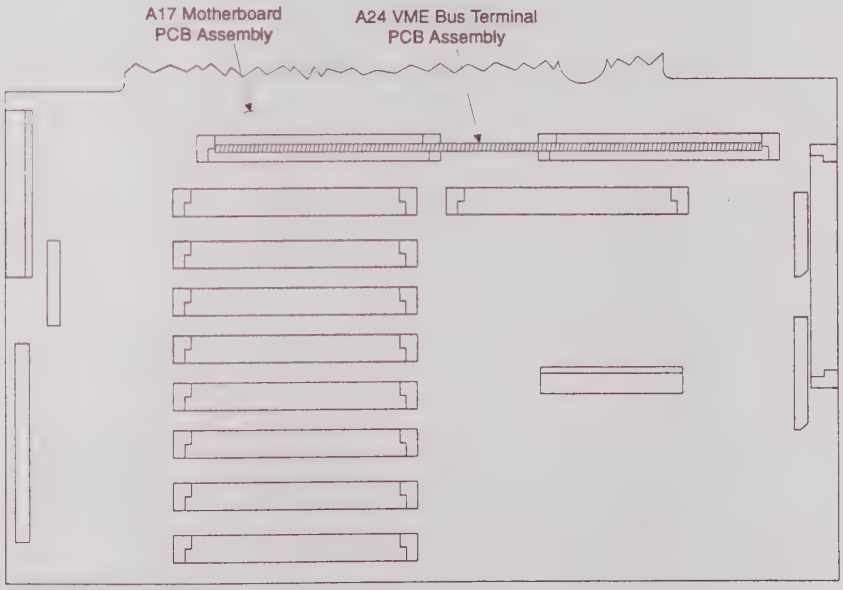


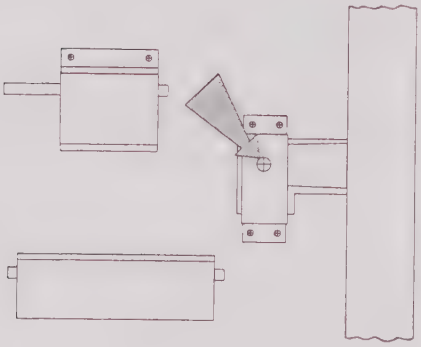

**Figure 8-5.** *Location of the A24 VME Bus Terminator PCB Assembly*

***Equipment Required:***

- ❑ Open-end wrench, 1 in.

***Preliminary:***

- ❑ Switch 373XXA power **off**. Remove the power cord.
- ❑ Remove handle assembles and all covers (paragraph 8-3).



***Remove/Replace Procedure:***

Step 1. Place the 373XXA in normal (top-side up) position.

Step 2. Remove the four corner screws and the top center screw that secure the front panel assembly to the chassis (see Figure 8-6).

Step 3. Place the 373XXA on its top (bottom-side up).

Step 4. Remove the screw that fastens the front panel casting extension lip to the Test Set Module tray. (See diagram at left.)

Step 5. Using a 1 in. open-end wrench, remove the nuts and washers that secure the Port 1 and Port 2 couplers/bridges to the front panel casting.

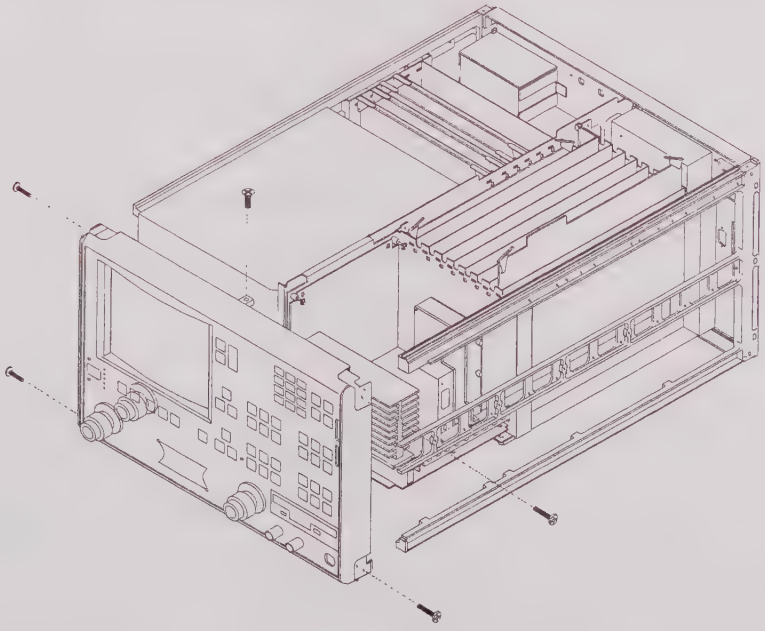


**Figure 8-6.** *Removal of Front Panel Assembly*

Step 6. Locate the cable from the front panel Power switch to connector J20 on the A17 Motherboard PCB. Disconnect at A17, J20 end.

Step 7. Locate the cable from the front panel Keyboard interface connector to connector J16 on the A17 Motherboard PCB. Disconnect at A17, J16 end.

Step 8. Locate the cables from the front panel Bias Input BNC connectors to connector P2 on the A18 Rear Panel PCB. Disconnect at A18, P2 end. (A18, P2 is the connector nearest to the bottom lip of the rear panel.)

Step 9. Gently pull front panel assembly several inches away from chassis. Locate cable from A17 Motherboard PCB to connector J1 on A20 Front Panel PCB. Disconnect at A20, J1 end.

Step 10. Separate the bias input cables (Step 8) from the cable harnesses, as necessary for removal. Pull front panel assembly free and set aside.

To replace the front panel assembly, perform the steps above in the reverse order.

## 8-9 VGA DISPLAY MONITOR

This paragraph provides instructions for removing and replacing the internal VGA Display Monitor assembly.

***NOTE***

It is not necessary to remove the front panel assembly to perform this procedure.

***Preliminary:***

- ❑ Switch 373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

***Remove/Replace Procedure:***

Step 1. Place the 373XXA on its right side (monitor down).

Step 2. At rear of monitor assembly, disconnect:

- The power cord (from the Power Supply Module)
- The data cable from motherboard CRT connector, J14
- The two cables from motherboard BRITE/DEGAUSS connector, J15.

***NOTE***

All the the cables mentioned above have keyed connectors.

Step 3. Remove the four screws that fasten the monitor assembly to the chassis (see Figure 8-7). Do **not** unfasten the screw with the blue plastic washer under the screw head.

Step 4. Gently move the monitor assembly to the rear and lift away from chassis, with cables still attached. Place on work surface next to unit.

To replace the Internal VGA Display Monitor assembly, perform the steps above in the reverse order.

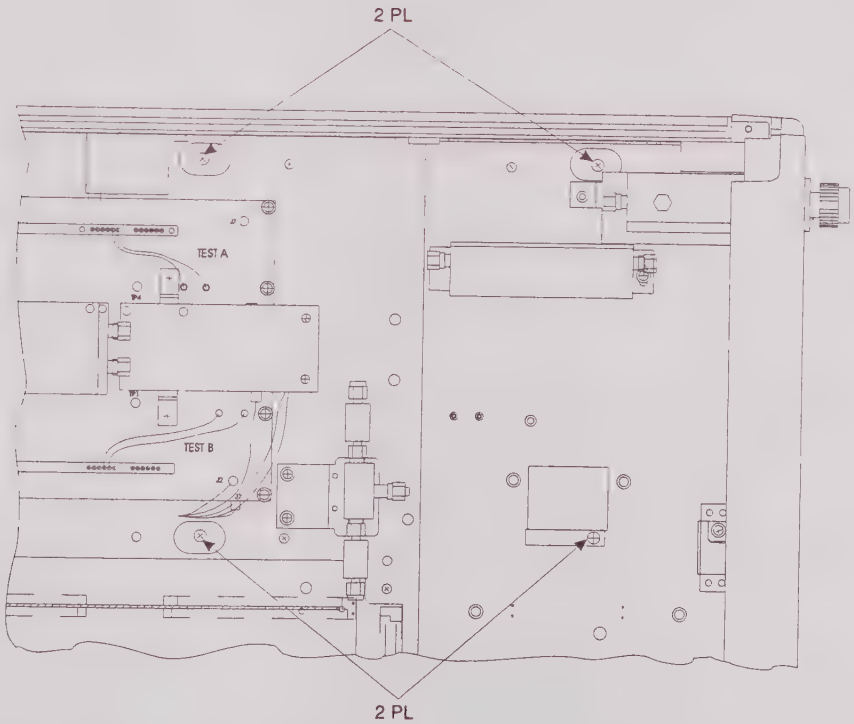



**Figure 8-7.** *Location of Internal VGA Monitor Assembly Mounting Screws*

## 8-10 LIQUID CRYSTAL DISPLAY (LCD)

This paragraph provides instructions for removing and replacing the internal LCD assembly.

***NOTE***

It is not necessary to remove the front panel assembly to perform this procedure.

***Preliminary:***

- ❑ Switch 373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

***Remove/Replace Procedure:***

Step 1. Place the 373XXA on its right side (monitor down).

Step 2. Disconnect the connector from LCD back light driver PCB Assembly and disconnect Flex PCB Assembly from LCD Assembly.

Step 3. Remove the four screws that fasten the monitor assembly to the chassis (see Figure 8-8).

Step 4. Gently move the monitor assembly to the rear and lift away from chassis.

Step 5. To replace the Internal LCD Monitor assembly, perform the steps above in the reverse order.

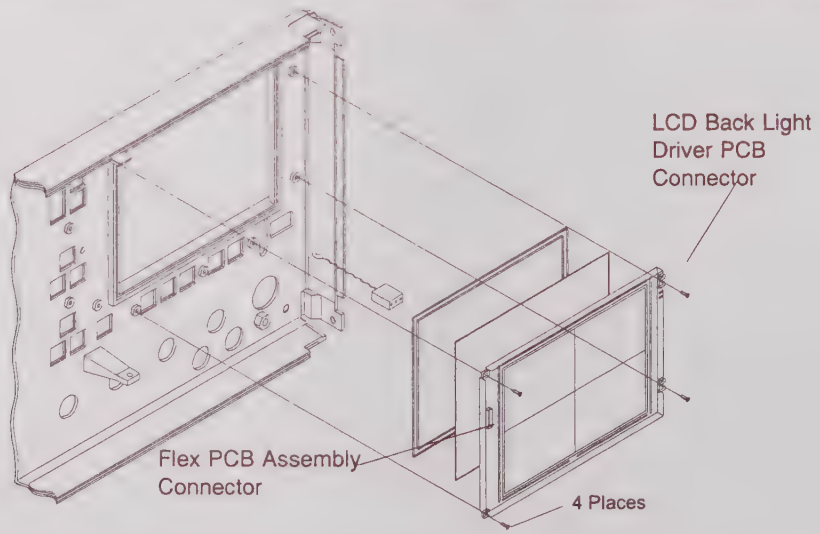



**Figure 8-8.** *Location of Internal LCD Assembly Mounting Screws*

## 8-10A LCD BACKLIGHT LAMP

This paragraph provides instructions for the removal and replacement of the LCD Backlight Lamp, which is recommended at approximately 10,000 hours of operation, or if the display becomes dim.

***NOTE***

The front panel assembly does not have to be removed.

***Preliminary:***

- ❑ Switch 373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

***Remove/Replace Procedure:***

Step 1. Remove the LCD assembly (paragraph 8-10).

Step 2. Remove the Backlight Lamp cover as follows:

On Sharp LQ9D169 LCD displays, remove the three Phillips screws on the side opposite the PCB, then lift off the cover.

On Sharp LQ9D340 LCD displays, on the side opposite the PCB, remove the tape covering the center catch. Starting at one end, very carefully push each catch clear of its tab while gently lifting the cover. Release all five catches and remove the cover.

Step 3. Carefull replace the Backlight Lamp, while being careful not to apply pressure to the area where the glass tube and the end caps of the Backlight Lamp meet.

Step 4. Reinstall the Backlight Lamp cover.

Step 5. Reinstall the LCD Assembly and reconnect electrical connectors.

Step 6. Reinstall the top cover.

Step 7. Turn the instrument on. Adjust the Brightness Potentiometer at the rear panel for maximum display brightness.

## 8-11 FLOPPY DISK DRIVE

This paragraph provides instructions for removing and replacing the Floppy Disk Drive assembly.

***NOTE***

It is not necessary to remove the front panel assembly to perform this procedure.

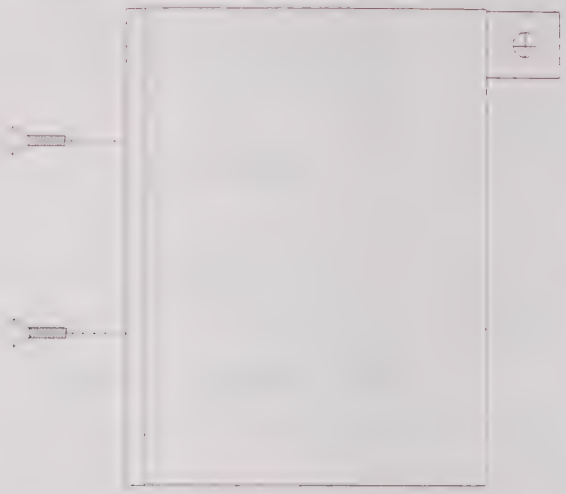


**Figure 8-9.** *Location of Floppy Disk Drive Assembly Mounting Plate Screws*

***Preliminary:***

- ❑ Switch 373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

***NOTE***

All the the cables mentioned in the following procedure have "keyed" connectors.

***Remove/Replace Procedure:***

Step 1. Place the 373XXA on its top (bottom-side up).

Step 2. At the floppy drive, disconnect the four-conductor Disk Power cable that connects to J1 of the motherboard PCB.

Step 3. At J2 on the motherboard PCB, disconnect the Floppy Control (ribbon) cable that goes to the floppy drive.

Step 4. Remove the three screws that fasten the floppy disk drive mounting plate to the chassis and to the Test Set Module tray (see Figure 8-9).

Step 5. Carefully pull the floppy disk drive assembly to the rear and up to remove assembly.

Step 6. Carefully remove the Floppy Control cable from the rear of the floppy drive. Set aside for re-use.

To replace the Floppy Disk Drive assembly, perform the steps above in the reverse order.

## 8-12 REAR PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the Rear Panel Assembly.

***Equipment Required Option 11 only):***

- ❑ Connector torque wrench (5/16 in), ANRITSU Model 01-201, or equivalent.

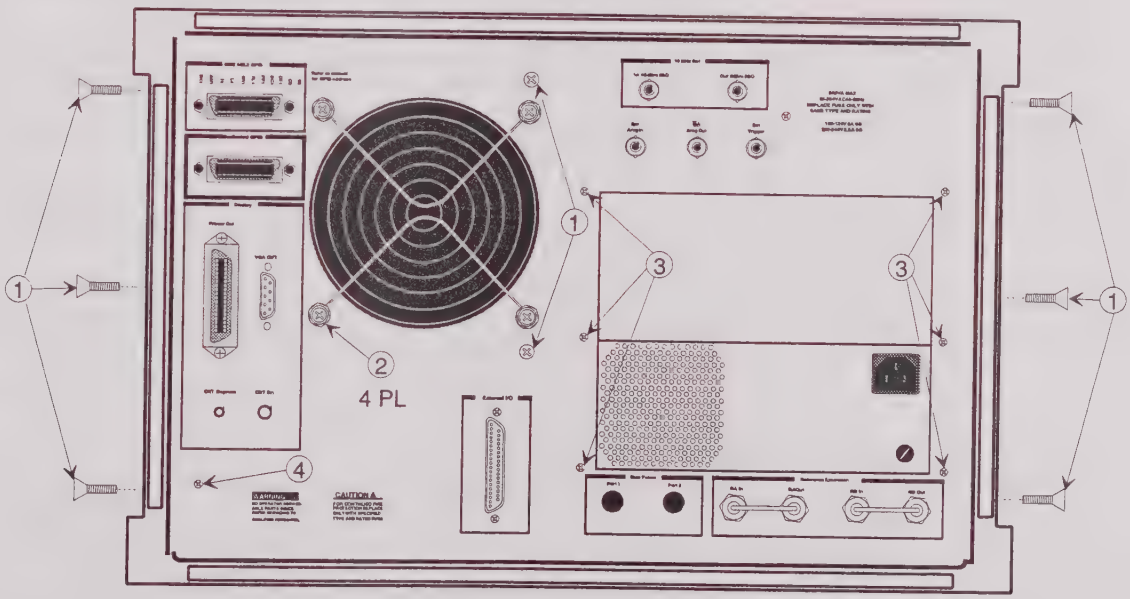
***Preliminary:***

- ❑ Switch 373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

***Remove/Replace Procedure:***

Step 1. Place the 373XXA in normal (top-side up) position.

Step 2. Remove the three screws on each side of the chassis that fasten to the rear panel assembly. See Figure 8-10.




①Rear Panel Assembly screws (par 8-11)
②Fan Assembly screws (par 8-12)
③Power Supply Assembly screws (par 8-13)
④A18 Rear Panel PCB screw (par 8-14)

**Figure 8-10.** *Location of Mounting Screws for Rear Panel Assemblies*

Step 3. Remove the two screws located near top and middle of rear panel (near fan-mounting screws). See Figure 8-10.

Step 4. Locate cable from the rear-panel 10 MHz Ref In BNC connector to connector J2 of A7 PCB. Disconnect at A7, J2 end. (Pull up gently to disconnect.)

Step 5. Locate cable from the rear-panel 10 MHz Ref Out BNC connector to connector J3 of A7 PCB. Disconnect at A7, J3 end.

Step 6. Locate cable from the rear-panel Ext Anlg In BNC connector to connector J1 of A5 PCB. Disconnect at A5, J1 end.

Step 7. Place the 373XXA on its right side (monitor down).

Step 8. Locate the cables from the rear-panel Ext Trigger and Ext Anlg Out BNC connectors to connector P13 of the A18 Rear Panel PCB. Disconnect at A18, P13 end. (A18, P3 is the fourth connector away from the rear panel bottom lip.)

Step 9. Disconnect the large ribbon cable from connector P1 of the A18 PCB at motherboard connector J12.

Step 10. Disconnect the two cables from the Power Supply Module at motherboard connectors J4 and J13.

Step 11. Disconnect power cord from the Power Supply Module to the internal VGA Display Monitor at the display monitor.

Step 12. If373XXA is equipped with Option 11, Reference Loop Extension Cables:

- Using a $\frac{5}{16}$ in. wrench, disconnect the external cable Loops from the rear panel connectors.
- Using a $\frac{5}{16}$ in. wrench, disconnect the semi-rigid coaxial lines W141 and W145 at the inside of the rear panel. See Figure 8-11 on page 8-23.

Step 13. If373XXA is equipped with Option 10, High Stability Time Base:

- Locate output cable from the high stability oscillator assembly (mounted above Power supply Module) to connector J1 of A7 PCB. Disconnect at A7, J1 end.
- Locate power cable from the high stability oscillator assembly to A17 Motherboard connector, J18. Disconnect at A17, J18 end.

Step 14. Place the373XXA in normal (top-side up) position. Gently pull rear panel assembly away from chassis and lay flat on

work surface. Remove cables from cable harnesses, as required.

To replace the Rear Panel Assembly, perform the steps above in the reverse order.

## 8-13 FAN ASSEMBLY

This paragraph provides instructions for removing and replacing the Rear Panel Fan Assembly.

***Preliminary:***

- ❑ Switch373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).
- ❑ Remove Rear Panel (paragraph 8-12).

***Remove/Replace Procedure:***

Step 1. Place the Rear Panel Assembly on the work surface with the A18 Rear Panel PCB up.

Step 2. Disconnect the two conductor fan power cable at connector P6 of the A18 PCB.

Step 3. Turn Rear Panel Assembly over, and remove the four screws that fasten the fan guard and fan assembly to the rear panel. See Figure 8-10.

Step 4. Remove the fan guard and separate the fan from the rear panel.

To replace the Rear Panel Fan Assembly, perform the steps above in the reverse order.

## 8-14 POWER SUPPLY MODULE

This paragraph provides instructions for removing and replacing the Power Supply Module.

***Preliminary:***

- ❑ Switch373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).
- ❑ Remove Rear Panel (paragraph 8-12).

***Remove/Replace Procedure:***

Step 1. Place the Rear Panel Assembly on the work surface with the Power Supply Module down.

Step 2. Remove the six screws from the rear panel that fasten it to the left and right edges of the Power Supply Module (see Figure 8-10). Gently separate the two units.

To replace the Power Supply Module, perform the steps above in the reverse order.

## 8-15 A18 REAR PANEL PCB

This paragraph provides instructions for removing and replacing the A18 Rear Panel PCB assembly.

***Equipment Required:***

- ❑ Nut Driver, 9/32 in.
- ❑ Nut Driver, 3/16 in.

***Preliminary:***

- ❑ Switch373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).
- ❑ Remove Rear Panel (paragraph 8-12).

***Remove/Replace Procedure:***

Step 1. Place the Rear Panel Assembly on the work surface with the A18 Rear Panel PCB up.

Step 2. Disconnect the two-conductor fan power cable at connector P6 of the A18 PCB.

Step 3. Disconnect the wiring for the rear panel Bias Fuses at connector P4 of the A18 PCB.

Step 4. Turn Rear Panel Assembly over. Remove screw located at lower left corner of the rear panel that fastens the A18 PCB to the Rear Panel Assembly (see Figure 8-10).

Step 5. Using a 9/32 in. nut driver, remove the standoffs that fasten the IEEE 488.2 GPIB and Dedicated GPIB connectors to the rear panel.

Step 6. Using a 3/16 in. nut driver, remove the standoffs that fasten the Printer Out, VGA Out, and External/IO connectors to the rear panel. Set standoffs aside for re-use.

Step 7. Carefully separate the A18 PCB from the rear panel.

To replace the A18 Rear Panel PCB assembly, perform the steps above in the reverse order.

## 8-16 TEST SET MODULE ASSEMBLIES

The following paragraphs provide instructions for removing and replacing the RF/microwave components that comprise the Test Set Module .

***Equipment Required:***

- ❑ Connector torque wrench (5/16 in), ANRITSU Model 01-201, or equivalent.
- ❑ Open-end wrench, 1 in.

***CAUTION***

Throughout these procedures, *always* use the 5/16 in. connector torque wrench for connecting the Test Set Module semi-rigid coaxial lines and RF/microwave components. Use of improper tools may damage the connectors, resulting in degraded instrument performance.

***Preliminary:***

- ❑ Switch373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

### *Transfer Switch*

Use the following procedure to remove/replace the Transfer Switch, which is common to all 373XXA models.

***Procedure:***

Step 1. For all models except 37269B: disconnect the semi-rigid coaxial line W87 from the input connector of the Transfer Switch. See Figure 8-11.

For Model 37269B: loosen the two screws that fasten the Transfer Switch mounting plate to the test set tray before disconnecting the semi-rigid coaxial line (W80). See Figure 8-12.

Step 2. Disconnect the Transfer switch.

Step 3. Carefully flex (do **not** bend) the rigid-coaxial lines to gain access to the lower connectors of the Transfer Switch; see Inset A on Figure 8-11. Remove rigid-coaxial lines from these connectors.

Step 4. Disconnect the Transfer Switch power cable at connector J5 of the A17 Motherboard PCB. Free the cable by separating it from the cable harness and by temporarily removing the A24 VME Terminator PCB.

Step 5. Remove the two screws that fasten the Transfer Switch mounting plate to the test set tray, and lift the Transfer Switch assembly from the Test Set Module.

To replace the Transfer Switch assembly, perform the steps above in the reverse order. W111 for Models 37211B and 37217B

***Input Coupler(s)/ Low Freq Bridge(s)***

Use the following procedure to remove/replace the Input Coupler(s) of all models 37225B through 37269B and the Low Frequency Bridges of models 37211B and 37217B.

***Procedure:***

Step 1. Using a 1 in. open-end wrench, remove the front panel nut and washer of the Port1or Port2 coupler/bridge that is to be removed.

Step 2. Disconnect the two semi-rigid coaxial lines associated with the coupler/bridge (see Figure 8-11).

Step 3. Remove the two screws that fasten the coupler/bridge bracket to the test set tray. Move coupler/bridge to the rear and up to remove it from the Test Set Module.

To replace the coupler/bridge, perform the steps above in the reverse order.

***Power Amplifier***

Use the following procedure to remove/replace the Power Amplifier assembly, which is common to all373XXA models.

***Procedure:***

Step 1. Disconnect the Power Amplifier power cable at connector J5 of the A17 Motherboard PCB. Free the cable by separating it from the cable harness and by temporarily removing the A24 VME Terminator PCB.

Step 2. Disconnect the PWR AMP IN cable on the side of the Power Amplifier assembly; see Figure 8-13. (Pull out gently to disconnect.)

Step 3. Remove the two screws that fasten the Power Amplifier assembly to the test set tray. Remove the two screws that fastens the assembly feet to the Buffer Amplifier/Sampler assembly.

Step 4. Disconnect the Power Amplifier from the Buffer Amplifier/Sampler by carefully pulling up on the connector end of the rigid-coaxial line from the Power Amplifier. (See Figure 8-13.) Carefully lift the assembly from the Test Set Module.

To replace the Power Amplifier assembly, perform the steps above in the reverse order.

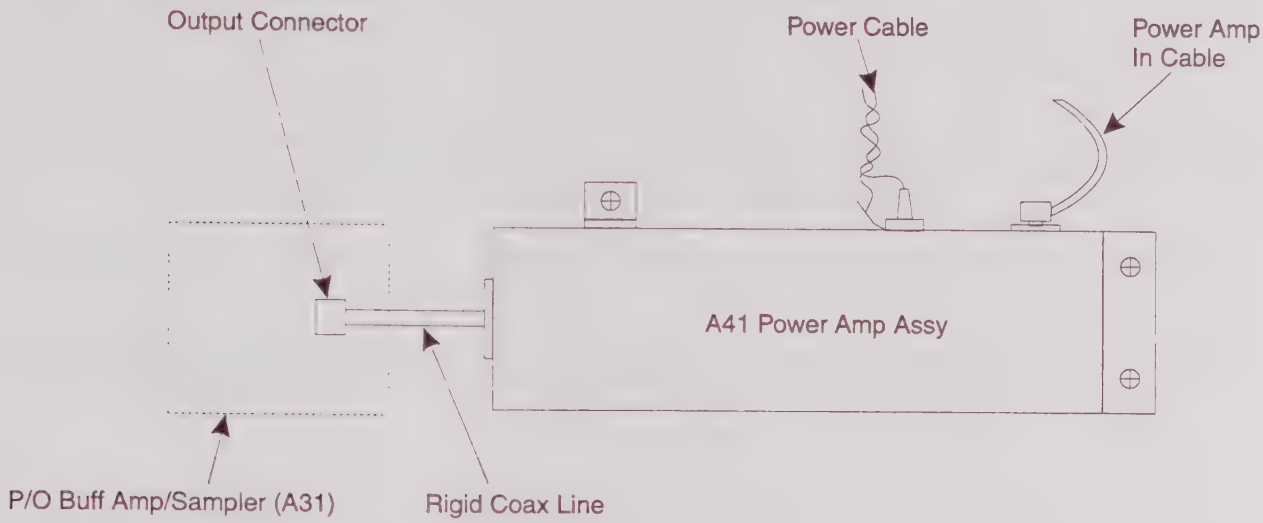



**Figure 8-13.** *A41 Power Amplifier Assembly, Details*

***Buffer Amplifier/ Sampler(A31)*** Use the following procedure to remove/replace the Buffer Amplifier/ Sampler assemblies of all models.

***Preliminary:***

❑ Remove the Power Amplifier assembly (see previous paragraph).

***Procedure:***

Step 1. Disconnect the semi-rigid coaxial lines, W83 and W84, from the 20 dB pads that are part of the Buffer Amplifier/Sampler assembly; see Figure 8-14. (For units with Option 11, the semi-rigid coaxial lines are W46 and W47.)

Step 2. Disconnect the cables from connectors J1 through J7 of the A31 Buffer Amplifier/Sampler assembly. (Pull up gently to disconnect.) Note that the connector end of each cable is marked with the associated A31 connector number.

Step 3. Disconnect the two cable connectors from the TEST A connector body on the Buffer Amplifier/Sampler assembly (see Figure 8-14). Similarly, disconnect the two cable connectors from the REF A connector body.

***NOTE***

The matching pin numbers are identified on the cable connectors and on the connector body.)

Step 4. Repeat Step 3 for the TEST B and REF B cable connectors.

Step 5. Remove the nine screws that fasten the Buffer Amplifier/Sampler assembly to the test set tray, and lift the assembly from the Test Set Module.

To replace the Buffer Amplifier/Sampler assembly, perform the steps above in the reverse order.

***Switched Doubler Module Assembly***

Use the following procedure to remove/replace the Switched Doubler Module (SDM) assembly for Model 37269B.

***Procedure:***

Step 1. Disconnect the SDM power cable from connector J17 of the A17 Motherboard PCB. Free cable from cable clip, as necessary.

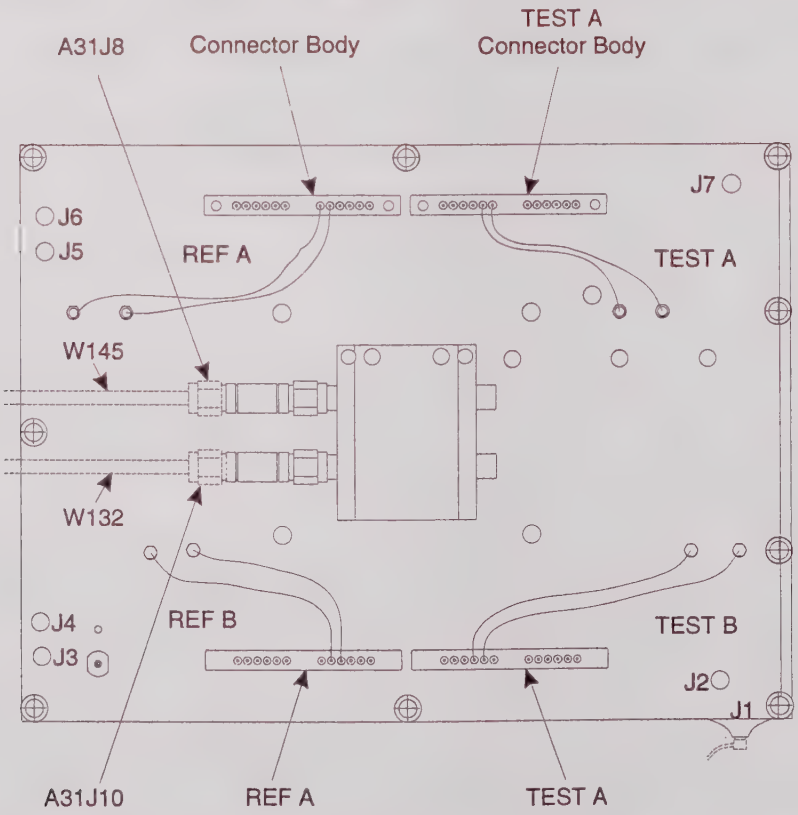



**Figure 8-14.** *A31 Buffer Amplifier / Sampler Assembly, Details*

Step 2. Disconnect the semi-rigid coaxial line W81 from the input connector of the SDM; see Figure 8-12.

Step 3. Remove the two screws that fasten the SDM to the Test Set Module tray.

Step 4. Disconnect the semi-rigid coaxial line W80 from the output connector of the SDM; see Figure 8-12. Carefully lift the assembly from the Test Set Module.

To replace the Switched Doubler Module assembly, perform the steps above in the reverse order.

## 8-17 SIGNAL SOURCE MODULES

The following paragraphs provide instructions for removing and replacing the RF/microwave components that comprise the Signal Source Module.

***Equipment Required:***

- ❑ Connector torque wrench (5/16 in), ANRITSU Model 01-201, or equivalent.

***CAUTION***

Throughout these procedures, *always* use the 5/16 in. connector torque wrench for connecting the Signal Source Module semi-rigid coaxial lines and RF/microwave components. Use of improper tools may damage the connectors, resulting in degraded instrument performance.

***Preliminary:***

- ❑ Switch373XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

***Removal of Signal Source Module***

Use the following procedure to remove the Signal Source Module from the chassis. This step is necessary before any of the module components can be removed/replaced.

***Procedure:***

Step 1. Place the373XXA on its top (bottom-side up).

Step 2. At J2 on the motherboard PCB, disconnect the Floppy Control (ribbon) cable that goes to the floppy drive. Dress the ribbon cable away from the Signal Source Module output connector; see Figure 8-11.

Step 3. Disconnect the semi-rigid coaxial line W87* from the output connector of the Signal Source Module.

Step 4. Place the373XXA in normal (top-side up) position.

Step 5. Disconnect the cables from connectors J1 and J2 of the A21A2 Source Control PCB. (Pull up gently to disconnect.) Note that the connector end of each cable is marked with the associated A21A2 connector number.

Step 6. Disconnect the cable from connector J3** of the A21A2 Source Control PCB. Dress cables away from the Signal Source Module.

Step 7. Remove the three screws that fasten the Signal Source Module to the chassis side rail. See Figure 8-15.

Step 8. Loosen the two captive screws that fasten the Signal Source Module to the chassis (Figure 8-15).

Step 9. Pull up at the rear of the Signal Source Module to disconnect the A21A1 Source YIG Bias Control PCB from the A17 Motherboard PCB. Lift the module from the chassis and place on work surface.

To replace the Signal Source Module, perform the steps above in the reverse order.

* W81 for Models 37269B

** Never operate unit with A21A2, J3 disconnected. Refer to Caution statement on

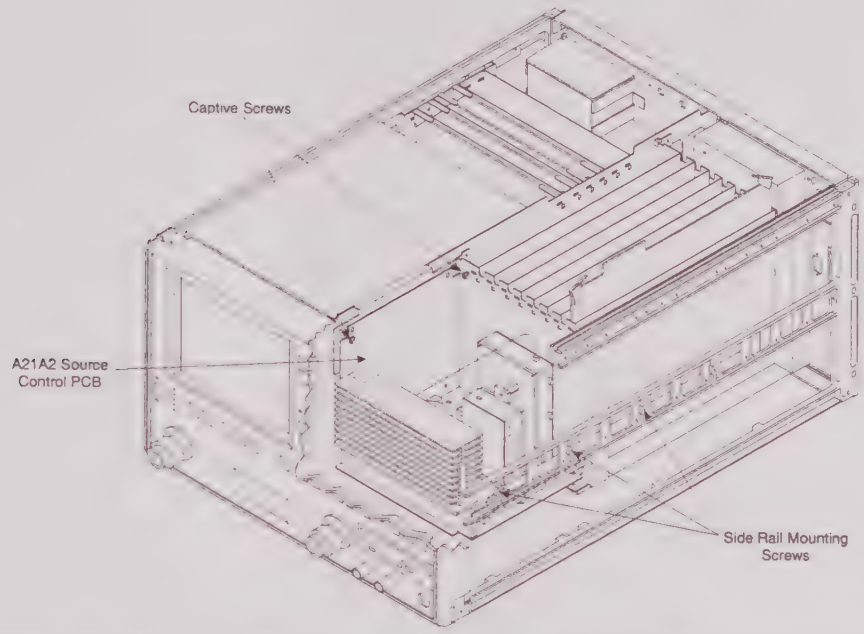



**Figure 8-15.** *Signal Source Module Removal Details*

***A21A2 Source Control PCB***

Use the following procedure to remove/replace the A21A2 Source Control PCB assembly.

***Procedure:***

Step 1. Unfasten the two PCB retainers at the top corners of the A21A2 Source Control PCB (see Figure 8-16). To unfasten, turn screwdriver slot ¼ turn *counter-clockwise*.

Step 2. Pull the top of the A21A2 PCB away from the source module chassis back plate to clear PCB retainers. Gently pull up to disconnect the A21A2 PCB from the socket on the A21A1 Source YIG Bias Control PC. Remove from Source Module.

To replace the A21A2 Source Control PCB assembly, perform the steps above in the reverse order.

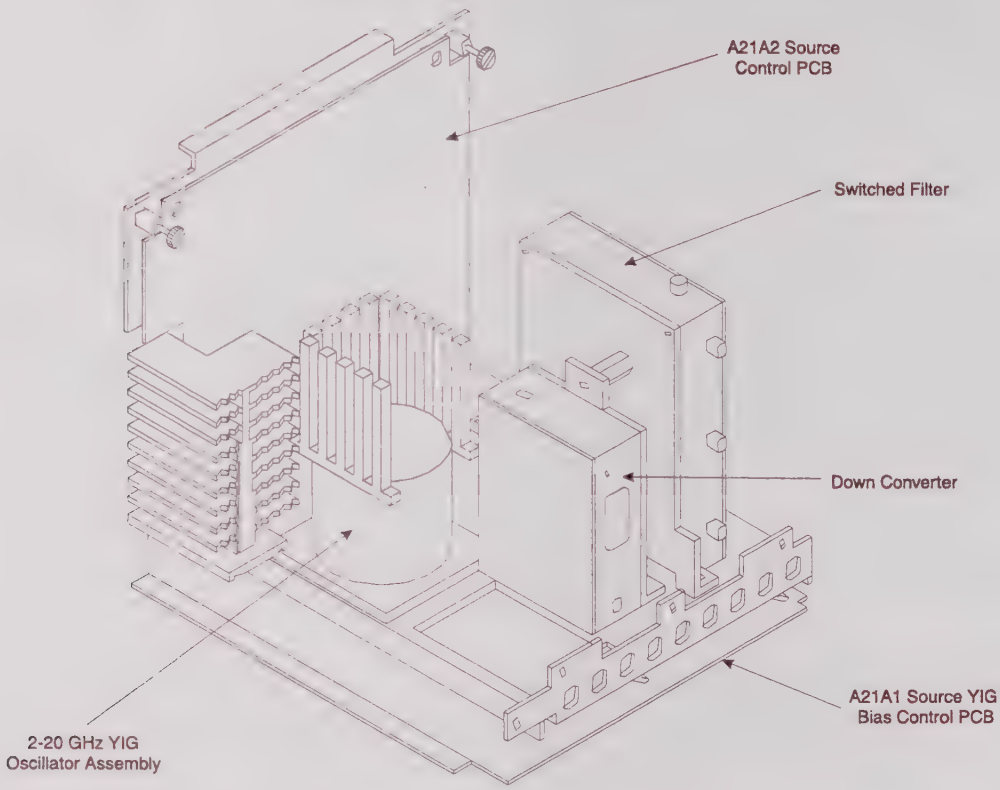



**Figure 8-16.** *Signal Source Module Assemblies Removal Details*

***A21A1 Source YIG Bias Control PCB***

Use the following procedure to remove/replace the A21A1 Source YIG Bias Control PCB assembly.

***Procedure:***

Step 1. Disconnect the Switched Filter assembly power cable from connector J1 of the A21A1 Source YIG Bias Control PCB. (Pull up gently on ribbon cable to disconnect.)

Step 2. Similarly, disconnect the Down Converter assembly power cable from connector J4 of the A21A1 PCB.

Step 3. Disconnect the YIG Oscillator assembly power cable from connector J3 of the A21A1 PCB. Pull up on the flexible circuit connector "handle" to disconnect.

Step 4. Remove the screw that fastens the front apron of the source module chassis to the heatsink of the A21A1 PCB. See Figure 8-16.

Step 5. Remove the four screws that fastens the back plate of the source module chassis to the heatsink of the A21A1 PCB.

Step 6. Place the Signal Source Module on its' back plate.

Step 7. Unfasten the six PCB retainers on the bottom of the A21A1 PCB. (To unfasten, turn screwdriver slot ¼ turn *counter-clockwise*.) Gently separate the A21A1 PCB (including the heat sink) from the Signal Source Module.

To replace the A21A1 Source YIG Bias Control PCB assembly, perform the steps above in the reverse order.

***Switched Filter Assembly***

Use the following procedure to remove/replace the Switched Filter assembly.

***Procedure:***

Step 1. Disconnect the power cable from connector P1 at the rear of the Switched Filter assembly. (Use a small screw driver to pry up gently at each end of the connector, as necessary.)

Step 2. Disconnect the semi-rigid coaxial lines from connector J6 (top) and connector J3 (lower-front) of the Switched Filter assembly.

Step 3. Disconnect the semi-rigid coaxial line from the RF INPUT (top) connector of the *Down Converter* assembly.

Step 4. Remove the two screws that fasten the Switched Filter assembly to the source module chassis and lift the assembly from the Signal Source Module.

Step 5. Disconnect the semi-rigid coaxial line from connector J1 (bottom) of the Switched Filter assembly. Put this coaxial line aside for re-use.

***NOTE***

When replacing the Switched Filter assembly, connect the semi-rigid coaxial line to the bottom connector (J1), before attaching the assembly to the Signal Source Module.

To replace the Switched Filter assembly, perform the steps above in the reverse order.

***Down Converter Assembly***

Use the following procedure to remove/replace the Down Converter assembly.

***Procedure:***

Step 1. Disconnect the power cable from connector P1 at the front of the Down Converter assembly.

Step 2. Disconnect the semi-rigid coaxial lines from the RF INPUT connector and RF OUTPUT connector of the Down Converter assembly.

Step 3. Remove the two screws that fasten the Down Converter assembly to the source module chassis and lift the assembly from the Signal Source Module.

To replace the Down Converter assembly, perform the steps above in the reverse order.

***YIG Oscillator Assembly***

Use the following procedure to remove/replace the YIG Oscillator assembly.

***Procedure:***

Step 1. Disconnect the YIG Oscillator assembly power cable from connector J3 of the A21A1 PCB. Pull up on the flexible circuit connector "handle" to disconnect.

Step 2. Disconnect the semi-rigid coaxial line from the connector J6 (top) of the *Switched Filter* assembly.

Step 3. Remove the four screws that fasten the YIG Oscillator assembly to the source module chassis and lift the assembly from the Signal Source Module.

Step 4. Disconnect the semi-rigid coaxial line from the output connector of the YIG Oscillator assembly. Put this coaxial line aside for re-use.

***NOTE***

When replacing the YIG Oscillator assembly, connect the semi-rigid coaxial line removed in Step 4 to the output connector of the YIG Oscillator before attaching it to the Signal Source Module.

To replace the YIG Oscillator assembly, perform the steps above in the reverse order.

# *Appendix A*
# *Diagnostics Menus*

## *Table of Contents*


| | | |
|---|---|---|
| A-1 | INTRODUCTION | A-3 |
| A-2 | DIAGNOSTICS MENUS | A-3 |
| | Start Self Test | A-3 |
| | Read Service Log | A-3 |
| | Installed Options | A-4 |
| | Peripheral Tests | A-4 |
| | Troubleshooting | A-4 |
| | H/W Calibrations | A-5 |

# *Appendix A*
# *Diagnostics Menus*

## *A-1* INTRODUCTION

This appendix contains descriptions and usage information for the 373XXA Diagnostic Menus that are available via the front panel Option Menu key.

## *A-2* DIAGNOSTICS MENUS

The internal diagnostic capabilities of the 373XXA are accessed via the Options Menu key, which is part of the front panel Enhancement key group. The selections available from the top level DIAGNOSTICS menu (DG1) are listed below. See Figure A-1.

- Start Self Test
- Read Service Log
- Installed Options
- Peripheral Tests
- Troubleshooting
- H/W Calibrations

### *Start Self Test*

The **START SELF TEST** selection, when invoked, will automatically test circuits throughout the 373XXA. Once invoked, it requires no external devices or interaction by the user. The net pass/fail result of the self-test is written to the CRT screen. Any self test failures will cause detailed failure information to be written into the service log.

This menu is available to service and non-service personnel.

### *Read Service Log*

The READ SERVICE LOG menu allows for viewing, printing, clearing, and saving the internal system service log to floppy disk. The **CLEAR LOG** function is not recommended for non-service personnel.

The Service Log is made up of two parts, the log header and the error listing. The log header contains key system parameters such as initial system turn-on date/time/temperature, current power-on date/time/temperature, total operational hours, system model, serial, and installed option numbers, date/time/temperature stamp of current service log viewing session, date/time/temperature of internal hardware calibrations, and statistics about various internal system phase locking activities.

The error listing is a time ordered log containing the system faults with details about the system condition at the time of the fault.

***NOTE***

The service log must always be printed out or saved to disk and sent to the factory along with a failed assembly. Due to the importance of the information provided by the service log to ANRITSU factory Service Engineers, the exchange prices are only valid if the service log data (disk or printout) is submitted to the factory with the failed assembly.

This menu is available to service and non-service personnel. However, the service log should be cleared by service personnel only.

***Installed Options***

The INSTALLED OPTIONS menu lists installed option numbers and descriptions.

This menu is available to service and non-service personnel.

***Peripheral Tests***

The PERIPHERAL TESTS menu (DG3) tests the printer and GPIB ports, internal VGA monitor, front panel operation, and the external IBM compatible keyboard (if keyboard is connected). These tests will require some interaction and external devices such as the Printer Test Connector (ANRITSU PN: B39553), a GPIB cable, and an external IBM compatible keyboard as appropriate for the specific test.

This menu is available to service and non-service personnel.

***Troubleshooting***

The TROUBLESHOOTING menu (DG4) and its sub-menus provide a host of pre-defined internal system modes and sub-system monitors that provide information useful in evaluating proper system operation. Most of these modes do not require any interaction or external test fixtures. (An exception is the FIRST IF BANDPASS selection which requires a thru line to be connected between the test ports.)

Menu DG4A and its sub-menus provide low level access to internal system hardware. These menus allow the user to control system latches, switches, and DACs. They also allow selection of key system states such as set-on or search for lock. Many internal analog voltages may be monitored via the 373XXA built-in DVM monitor network.

***CAUTION***

Always exit the troubleshooting mode via the DG4 menu selection **FINISHED, RECOVER FROM TROUBLE-SHOOTING** to insure proper system state recovery from your troubleshooting activities.

These menus are for service personnel only.

***H/W Calibrations***

The H/W CALIBRATIONS menus perform various internal automated hardware calibrations, including ALC and Frequency calibrations. The following equipment is required for these tests:

- HP 437B Power Meter (or Gigatronics 8541/42 Power Meter)
- ANRITSU ML24XXA with Version 2.02 or later, with ANRITSU Power Sensors MA2474A and (TCD) for 65 GHz units.
- EIP 20 GHz series counter w/ GPIB (Option -08)

You need only connect the power meter or counter appropriate for the 373XXA model, invoke the calibration desired, and wait until complete. The ALC and Frequency calibrations take 5 to 10 minutes each. See Chapter 6, Adjustments, for further information.

The disk operations allow storage and retrieval of internal hardware calibration data to and from floppy disk. This feature will be useful when replacing the A9 Processor PCB since it contains the Battery Backed RAM where the internal hardware calibration data resides.

Automated field calibrations for the LO1 and LO2 assemblies are not presently implemented. Should these assemblies fail or require any adjustment, they must be replaced under the exchange assembly program (refer to Chapter 1).

These menus are for service personnel only.

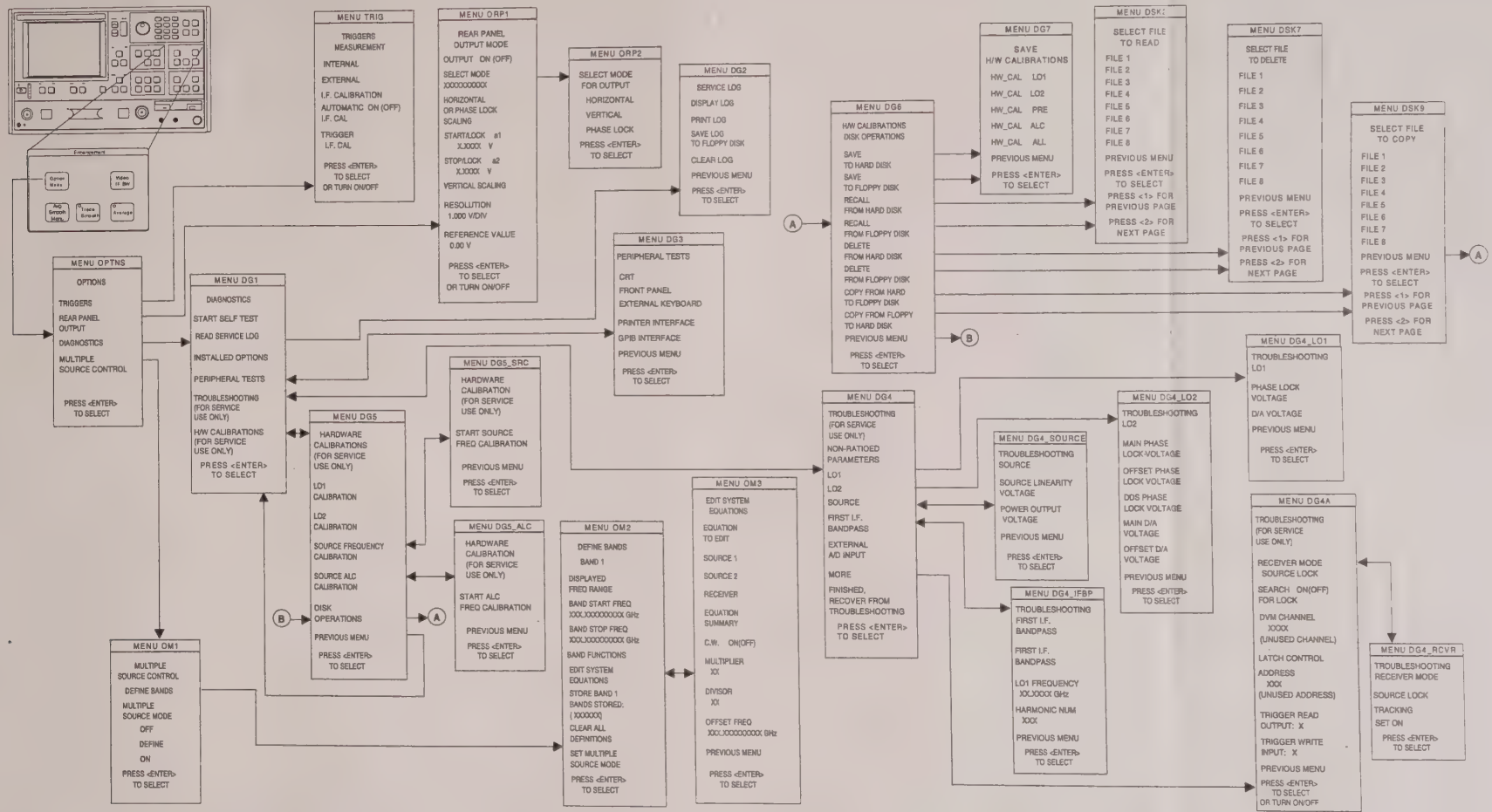



*Figure A-1. Diagnostics Menus*

# *Appendix B*
# *Error Messages*

## *Table of Contents*


| | | |
|---|---|---|
| B-1 | INTRODUCTION | B-3 |
| B-2 | OPERATIONAL ERROR MESSAGES | B-3 |
| B-3 | DISK RELATED ERROR MESSAGES | B-3 |
| B-4 | GPIB RELATED ERROR MESSAGES | B-3 |
| B-5 | SERVICE LOG ERROR MESSAGES | B-3 |
| | 0000 - 0099 | B-3 |
| | 0100 - 3999 | B-3 |
| | 4000 - 4999 | B-4 |
| | 5000 - 5999 | B-4 |
| | 6000 - 6999 | B-4 |
| | 7000 - 7999 | B-4 |
| | 8000 - 8999 | B-4 |

# *Appendix B*
# *Error Messages*

## B-1 INTRODUCTION

This appendix provides a listing of error messages that appear on the 373XXA display or that are written to the internal software Service Log.

## B-2 OPERATIONAL ERROR MESSAGES

Table B-1 provides a listing and description of the operational error messages. For the most part, these errors are displayed only on the 373XXA display and are caused by incorrectly operating the 373XXA.

## B-3 DISK RELATED ERROR MESSAGES

Table B-2 provides a listing and description of the disk-related-error messages. The numbered errors in this group are also written to the Service Log, since they may indicate system problems.

## B-4 GPIB RELATED ERROR MESSAGES

Table B-3 provides a listing and description of GPIB-related error messages. These errors are entered in the Service Log and output as part of the response of OGE/OGL commands.

## B-5 SERVICE LOG ERROR MESSAGES

Table B-4 provides a listing of the error messages that are written to the internal system service log. Some of these messages may occur as a result of incorrectly programming the 373XXA. This includes the GPIB errors, 7204–7207, and errors in the 5000 range, RF Power. The RF Power errors may be triggered when setting the 373XXA power to a value greater than its reset level. This feature of the 373XXA lets you take advantage of all available power; however, accuracy cannot be guaranteed when power is unleveled. Refer to Chapter 5, paragraph 5-6 for additional guidance in interpreting these error codes.

The error messages in Table B-4 are numbered and organized as follows:

***0000 - 0099*** These messages generally indicate status or a pass/fail result of a Peripheral or Self test.

***0100 - 3999*** These messages primarily indicate a self-test failure with the suspect assembly number being the two high-order digits. For example, error 0111 indicates test 11 for the A1 assembly has failed, similarly, error 0814 is related to the A8 assembly test #14, and error 2138 is related to the A21 assembly test #38.

Since these errors are primarily self-test errors, they do not get displayed but only get written to the service log. Any exceptions to this

rule will be an assembly error code between xx00 - xx09, where xx is the assembly that is suspected of failing during normal operation. For example, error 0500 is a run-time error related to the A5 A/D assembly.

***4000 - 4999*** These messages indicate internal H/W calibration problems.

***5000 - 5999*** These messages indicate run-time RF power problems.

***6000 - 6999*** These messages indicate run-time phase lock problems. A letter or sequence of letters following the error message depict the suspect assembly(ies) as follows:

- A = 10 MHz Reference
- B = LO1 unlocked
- C = LO2 unlocked
- D = Source unlocked
- E = IF lock signal level too low
- F = External synthesizer unlocked
- G = LO3 unlocked
- None = Unknown

***7000 - 7999*** These messages indicate a run-time digital section problem.

***8000 - 8999*** These messages indicate a run-time processing system problem.

***Table B-1.*** *Operational Error Messages (1 of 2)*

| Error Message | Description | Corrective Action |
|---|---|---|
| ATTENUATOR UNAVAILABLE | Option 6 Port 2 Test Step Attenuator is not installed. | Install Option 6 Step Attenuator, |
| DIFFERENT H/W SETUP. RECALL ABORTED | Model and/or options is (are) different from the recalled setup. | Reconfigure system to duplicate the hardware setup that was used to store the saved data. |
| DIFFERENT S/W VERSION, RECALL ABORTED | Saved state not compatible with software version or options. | Load compatible software (S/W) version and retry. |
| FREQUENCIES HAVE REACHED UPPER LIMIT | Frequencies being defined in Multiple Source mode have reached upper limits of Sources. | Redefine frequencies to not exceed limits of Sources. |
| MEMORY LOCATION CORRUPTED | Requested memory location is corrupted. | None. If problem reoccurs after storing a new setup, contact ANRITSU Customer Service. |
| NO BANDS ARE STORED | No frequency bands have been defined and stored. | Define and store frequency bands to turn on Multiple Source mode. |
| NO STORED MEMORY DATA | No data is stored in memory for display or trace math. | Store or re-save measurement data. |
| OPTION NOT INSTALLED | Selected an option that is not installed. | None. |
| OUT OF CAL RANGE | Entered values out of the selected calibration range. | Change calibration range or re-enter values that are within the current range. |
| OUT OF H/W RANGE | Entered value is out of the instrument's hardware range. | Re-enter values that are within range. |
| OUT OF RANGE | Entered value is out of range. | Re-enter values that are within range. |
| RECEIVER OUT OF RANGE BY EQUATION | Equation defined in Multiple Source mode places receiver frequency out of range when attempting to store band. | Redefine frequency. |
| SOURCE 1 OUT OF RANGE BY EQUATION | Equation defined in Multiple Source mode places Source 1 frequency out of range when attempting to store band. | Redefine frequency. |
| SOURCE 2 OUT OF RANGE BY EQUATION | Equation defined in Multiple Source mode places Source 2 frequency out of range when attempting to store band. | Redefine frequency. |

*Table B-1. Operational Error Messages (2 of 2)*

| Error Message | Description | Corrective Action |
|---|---|---|
| STANDARD CAL NOT VALID FOR WAVEGUIDE | Cannot use the standard method when calibrating with waveguide. | Use the Offset Short method with waveguide. |
| START F FOLLOWS PREVIOUS STOP F | Start frequency of current band immediately follows stop frequency of previous band. Cannot be modified. | None. |
| START MUST BE LESS THAN STOP | Entered start frequency is greater than the stop frequency. | Re-enter frequency values such that the start frequency is lower than the stop frequency. |
| STEP IS TOO LARGE | Entered harmonic frequency extends the stop out of range. | Re-enter so that harmonic frequency is within range. |
| STOP IS OVER RANGE | Entered value exceeds the instrument's stop frequency. | Re-enter stop frequency. |
| SYSTEM NOT CALIBRATED | 373XXA is uncalibrated for the selected measurement values. | Perform a measurement calibration. |
| TOO FEW POINTS, 2 MINIMUM | Entered too few discrete fill points, 2 is minimum. | Re-enter data points. |
| TOO MANY POINTS, 1601 MAXIMUM | Entered too many discrete fill points, 1601 points are the maximum allowed. | Re-enter data points. |
| UNDEFINED DIVIDE BY ZERO | Denominator cannot be zero in equation. | Make denominator a value other than zero. |
| WINDOW TOO SMALL | Attempted to set time domain range smaller than allowed | Re-enter larger time range. |
| OUT OF WINDOW RANGE | Attempted to set time domain range larger than allowed | Re-enter values within allowed range. |

***Table B-2.*** *Disk-Related-Error Messages (1 of 1)*

| Error Message | Description | Corrective Action |
|---|---|---|
| 7140 GENERAL FLOPPY DRIVE FAIL | Invalid disk media or format. | Use 1.44 MB diskette and/or format in the 373XXA. |
| 7142 FLOPPY DISK READ ERROR | Read error when accessing disk file. | Use 1.44 MB diskette and/or format in the 373XXA. |
| 7143: FLOPPY DISK WRITE ERROR | Error in writing to disk file. | Use 1.44 MB diskette and/or format in the 373XXA. |
| 7147 FLOPPY DISK UNAVAILABLE | Floppy disk is not available. | Install floppy diskette and/or check floppy disk drive. |
| 7170: GENERAL HARD DISK FAIL | General error in accessing hard disk. | Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive. |
| 7172: HARD DISK READ ERROR | Read error when accessing disk file. | Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive. |
| 7173: HARD DISK WRITE ERROR | Error in writing to disk file. | Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive. |
| 7177: HARD DISK UNAVAILABLE | Hard disk is not available. | Install hard disk drive and/or check operation of hard disk. |
| 8140: GENERAL DISK BUFFER ERROR | Out of RAM. | Press the System State, Default Program key, and retry. This will reset the 373XXA to the factory default state. |
| FILE NOT FOUND | Disk file not found. | None. |
| FLOPPY DISK HAS NO ROOM FOR FILE | Floppy diskette is full. | Delete files or install new diskette. |
| FLOPPY DISK NOT READY | Floppy disk is not ready (or not installed.). | Install diskette in floppy drive. |
| FLOPPY DISK WRITE PROTECTED | Write protect tab in place on floppy diskette. | Remove write-protect tab. |
| HARD DISK HAS NO ROOM FOR FILE, DELETE EXISTING FILES(S) TO CREATE SPACE | Hard disk is full. | Delete unneeded files. |

*Table B-3. GPIB-Related Error Messages (1 of 8)*

| Error Message | Description |
|---|---|
| These errors are entered in the Service Log and output as part of the response of OGE/OGL commands for GPIB commands. The list is subdivided into the type of GPIB error: 7204..., 7205..., 7206..., and 7207. | |
| | 7204 GPIB COMMAND ERROR DESCRIPTIONS |
| Faulty program mnemonic syntax | Generated when the program mnemonic found was not one of the currently defined program mnemonics for the 373XXA. |
| Faulty suffix mnemonic syntax | Generated when the suffix mnemonic found was not one of the currently defined suffix mnemonics for the 373XXA. |
| Faulty mnemonic syntax | Generated when the mnemonic found was not one of the currently defined program or suffix mnemonics for the 373XXA. |
| Missing Program Message Separator | Generated when the required semicolon preceding the next program mnemonic was not found. |
| Expected NRf data | Generated when a mnemonic is used that requires a trailing NRf numeric data element. The data element was either missing or the first character of the data element was not one of the acceptable NRf characters. |
| NRf mantissa too long | The maximum allowable number of characters in the NRf numeric element mantissa is 255. |
| Exponent magnitude too large | The maximum allowable exponent magnitude in an NRf element is +/— 32000. |
| Faulty NRf syntax | Can be any number of syntactical errors such as more than one decimal point, inclusion of a decimal point in the exponent field, an invalid character imbedded in the numeric or no exponent value following the 'E'. |
| Expected String Program Data | Generated when a mnemonic is used that requires a trailing string data element. The date element was either missing or no open quote character was found. |
| Missing close quote character | Generated when a mnemonic is used that requires a trailing string data element. The open quote character was found, but the close quote character was not. |
| Expected Arbitrary Block data | Generated when a mnemonic is used that requires a trailing arbitrary block data element and the trailing element was not an arbitrary block data element. Or in some cases, the arbitrary block was empty. |
| Faulty Arbitrary Block | Generated when a defined length arbitrary block data element is terminated early with an EOI or an indefinite length arbitrary block data element is not properly terminated. |
| Missing Program Data Separator | Two data elements of a program mnemonic that requires multiple program data elements, are not properly separated from each other by a comma. |

***Table B-3.*** *GPIB-Related Error Messages (2 of 8)*

| Error Message | Description |
|---|---|
| GET received during PM reception | Generated when the GPIB Command 'Group Execute Trigger' is received during the reception of a program message but before its proper termination with the end message. The partial program message up to but not including the 'Group Execute Trigger' will be executed. Execution of the Group Execute Trigger and any subsequent program message elements received before the end message will be skipped. |
| | 7205 GPIB EXECUTION ERROR DESCRIPTIONS |
| Not permitted in a DDT command sequence | When executing a defined device trigger command sequence, a forbidden command was detected. |
| Too much Arbitrary Block data | The arbitrary block supplied contained more data than was necessary for the currently defined 373XXA state. This can occur when graph types, start/stop frequencies or data points are changed. |
| Insufficient Arbitrary Block data | The arbitrary block supplied did not have enough data for the currently defined 373XXA state. This can occur when graph types, start/stop frequencies or data points are changed. |
| Invalid parameter for current graph type | An attempt was made to program a non-existent parameter for the current graph type. For instance, a Smith chart does not have a reference or reference line position (mnemonics OFF and REF). |
| Parameter out of range | An attempt was made to program an out of integer range value for a parameter. This error is detected by the GPIB MANAGER when converting and rounding to the appropriate integral size (signed/unsigned char/short or long). |
| Parameter value not permitted | A parameter value was not found in the list of permissible values for that parameter. |
| CW marker sweep not permitted in time domain | The mnemonics M1C, M2C, M3C, M4C, M5C and M6C are forbidden in time domain. |
| Parameter unavailable in frequency domain | The mnemonic ODV and OTV are forbidden in frequency domain. |
| Port 2 Test Attenuator (OPT 6) not installed | The mnemonic TA2 is forbidden when the attenuator is not installed. |
| Time Domain (OPT 2) not installed | An attempt was made to use one of the time domain mnemonics when the option is not installed. |
| Return to Local not permitted in Local Lockout | The mnemonic RTL failed due to being in the Local Lockout mode. |
| Calibration does not exist | An attempt was made to turn on flat power correction or vector error correction when the corresponding calibration does not exist. |
| Cal term not available | An attempt was made to get a calibration term which does not exist for the current calibration type. |

*Table B-3. GPIB-Related Error Messages (3 of 8)*

| Error Message | Description |
|---|---|
| Invalid cal term for calibration type | An attempt was made to program a calibration term which does not exist for the current calibration type. |
| Front panel setup not valid | An attempt was made to get a front panel setup that did not contain a correct/valid state. |
| Normalization data not valid | An attempt was made to reference normalization data when there was no normalization data currently stored. |
| Command sequence too long | An attempt was made to define a device trigger command sequence which had more than 255 characters. |
| Unable to display menu | An attempt was made to display a menu which could not be displayed for the current 373XXA state. |
| String too long | An attempt was made to enter a string for the following mnemonics which exceeded the specified maximum length.<br><br>LTD, LID, LMS and LNM - maximum length is 15 characters.<br><br>LOC - maximum length is 79 characters. |
| Must specify a calibration type first | In order to perform a calibration, the calibration type must be specified by the use of one of the Cxx mnemonics (i.e. C12, C8T, etc.) PRIOR to the issuance of the mnemonics CWC, TDC or BEG. |
| Parameter value unchanged | An attempt was made to change a start/stop frequency or number of data points to a value outside of the current calibrated range with correction turned on. |
| Parameter change not permitted | An attempt was made to perform an illegal state change or action based on the current 373XXA state. This includes attempting to store an undefined band definition. Or certain changes from the calibration state or the calibration define state when defining discrete frequencies. |
| Parameter value out of range<br>Parameter out of hardware range | An attempt was made to set a parameter to a value outside of the permissible range of values for the parameter. |
| Standard cal method not valid for waveguide | In a waveguide type of calibration, the standard (OSL) cal method is forbidden. |
| Out of calibrated range | An attempt was made to change a parameter not permitted to be changed with correction on. |
| Start must be must be less than stop | An attempt was made to set a new start frequency, distance or time greater than or equal to the current stop frequency, distance or time. Or to set a new stop frequency, distance or time less than or equal to the current start frequency, distance or time. |
| Tune mode requires a 12 term calibration | Perform a 12 term calibration prior to turning on tune mode. |

*Table B-3. GPIB-Related Error Messages (4 of 8)*

| Error Message | Description |
|---|---|
| Current and cal frequencies different | The flat power calibration setup does not match the current setup. |
| Stored data is invalid | An attempt was made to reference normalized data when normalized data was invalid. |
| Parameter change not permitted on current state | An attempt was made to change a parameter while IF cal was active. It is not expected that this message will ever be seen. If you see this message, notify the factory. |
| Calibration may not be valid | An attempt was made to repeat the previous calibration when there was no record of a previous calibration. |
| Calibration does not exist | An attempt was made to turn on flat power correction or vector error correction when the corresponding calibration does not exist. |
| Current calibration is erased | When turning on Multiple Source Mode with vector error correction on, the calibration is destroyed. Not really an error. Message is issued as a warning. |
| Time Domain and CW mode not permitted | An attempt was made to turn on a time domain mode in CW. This is not permitted. |
| Not permitted in Time Domain | An attempt was made to select a group delay display or CW mode when in time domain mode or to select a dual overlay display with a frequency/time domain mismatch. |
| Time Domain not allowed | An attempt was made to turn on a time domain mode but the current 373XXA state does not permit it. |
| Permitted only in diagnostic mode | Must put the 373XXA into the diagnostics mode via the SDG command before using this mnemonic. |
| Graph types not appropriate for dual overlay | While in dual overlay mode, and attempt was made to change one of the active graph types to a type which conflicts with dual overlay, or to change one of the active channels into or out of time domain which sets up a dual overlay conflict. Or an attempt was made to select dual overlay mode when there would be a graph type conflict for a frequency/time domain conflict. |
| New Discrete Fill not allowed in current state | Cannot set up a new discrete fill definition while performing a calibration or when correction is turned on. Also cannot do this when group delay is the graph type on the active channel. |
| Low Pass mode requires a harmonic sweep | Perform a TD harmonic sweep calibration prior to using this mnemonic. |
| Receiver out of range by equation | Problems with the internal source, external source or receiver equations in multiple source mode. |
| New start less than previous stop | An attempt was made to set the start frequency for the new multiple source mode band definition to a frequency less than the stop frequency of the previous band. |

*Table B-3. GPIB-Related Error Messages (5 of 8)*

| Error Message | Description |
|---|---|
| Bad filename | The supplied filename was bad. The filename can have 8 characters maximum. No extensions. The filename must start with and alpha type character (A thru Z). After that the allowable characters are alpha, numeric (0 thru 9) and underscore (_). |
| Conflict with rotary knob | You should not be using the rotary knob and the GPIB at the same time. |
| Too many data points for external source | A 6700B series external source can handle 501 data points.<br>A 68000 series external source can handle 999 data points. |
| Recalled setup corrupted<br>Hardware mismatch in recalled setup<br>Software mismatch in recalled setup | These are problems with the recalled setup. |
| Too many data points for Discrete Fill | The maximum number of data points in discrete fill is 1601. |
| Not enough data points for Discrete Fill | The minimum number or data points in discrete fill is 2. |
| Discrete Fill end frequency out of range | The number of points for discrete fill puts the end frequency out of range. |
| Step is too large | When setting up a time domain harmonic sweep, cannot get 2 data points because the start frequency is too high for the approximate stop frequency. In a group delay display, the delay aperture percent of sweep is less than one step size. |
| Range too small | An attempt was made to set a distance or time span value too small. This can also be done via inappropriate values for start and stop. |
| Start or stop out of range | An attempt was made to set a distance or time start or stop value out of range. This can also be done via inappropriate values for center and span. |
| No bands defined | An attempt was made to turn on multiple source mode with no band definitions. |
| Out of frequencies for new band definition<br>Source out of range by equation<br>External source out of range by equation | The current set of multiple source mode bands use up all the frequency range of the 373XXA. Therefore, no more bands can be defined. |
| File is read only | An attempt was made to write to a write protected file. |
| File not found | An attempt was made to access a non-existent file. |
| Floppy drive not ready | An attempt was made to access the floppy drive with no floppy disk installed. |
| Floppy disk full<br>Hard disk full | An attempt was made to write to a floppy disk or the hard disk when no space was left on the disk. |

*Table B-3. GPIB-Related Error Messages (6 of 8)*

| Error Message | Description |
|---|---|
| Floppy disk write protected | An attempt was made to write to a write protected floppy disk. |
| Recalled setup or data file corrupt | An attempt to recall a setup from internal memory, the GPIB or disk failed due to software revision or hardware mismatch or checksum error. |
| New frequency list not allowed in current state | Cannot set up a new discrete fill definition while performing a calibration or when correction is turned on. Also, cannot do this when group delay is the graph type on the active channel. |
| State change not permitted | An attempt was made to perform an illegal state change or action based on the current instrument state. This includes attempting to store (1) an undefined band definition, (2) certain changes from the calibration state, or (3) the cal define state when defining discrete frequencies. |
| Faulty label or file name | The label or file name associated with the current mnemonic is faulty. |
| Illegal characters in filename | The first character in a filename must be an alpha type. The remaining characters can be alpha, numeric, or underscores. An extension is not permitted. |
| Filename too long | The maximum lednqth for filenames is 8 characters. An extension is not permitted. |
| Floppy disk read error<br>Floppy disk write error<br>Hard disk read error<br>Hard disk write error | Read or write error(s) occurred while attempting to access the indicated disk. |
| Floppy disk not found<br>Hard disk not found<br>General disk buffer error<br>General floppy drive failure<br>Floppy disk init failure<br>General hard disk failure<br>Hard disk control failure<br>Hard disk init failure<br>Unknown disk error | Other error messages which suggest that the indicated drive is in need of service. |
| 7205 GPIB QUERY ERROR DESCRIPTIONS | |
| No Response data available | Generated if the controller attempts to read response data from the 373XXA and none is available. |
| No Response data after PM completion | This is the same as the 'no response data available' case above except that a program message was currently being parsed and executed when the controller attempted to read data. Detection of this error was deferred until the parser/execution block was finished with the current program message and it was observed that no response data was generated. |

*Table B-3. GPIB-Related Error Messages (7 of 8)*

| Error Message | Description |
|---|---|
| Response after Indefinite Response discarded | This error is generated when the 373XXA's output queue has already received an Arbitrary ASCII response data element and an attempt is made to place another response data element of any kind into the queue. The new response data element is discarded. |
| Interrupted - Response data discarded | This error is detected when the output queue contains unread response data and the controller sends a new program message. The response data is discarded. |
| Unterminated - Partial PM will be executed | This error is detected when the 373XXA's input queue is currently receiving a program message but has not yet received the end message, and the controller attempts to read response data from the 373XXA. The partial program message in the input queue is executed as if it were properly terminated. |
| Deadlock - Response data discarded | This error is detected when both of the 373XXA's input and output queues are full and the controller attempts to send another data byte. In order to prevent bus deadlock, the contents of the output queue are discarded. |
| | 7205 GPIB DEVICE DEPENDENT ERROR DESCRIPTIONS |
| Q_SEND failure in [a procedure name] | An unsuccessful attempt was made to send a message to a task.<br><br>The procedure name is the place in the software where the error was detected. |
| Q_RECEIVE failure in [a procedure name] | A failure was detected while waiting for the reception of a message from a task.<br><br>The procedure name is the place in the software where the error was detected. |
| Unable to allocate memory in [a procedure name] | An attempt was made to allocate some temporary memory in order to accomplish a task directed in the program message.<br><br>The procedure name is the place in the software where the error was detected. |
| Unable to release memory in [a procedure name] | An attempt was made to return some temporary memory within a task and the return failed for some reason.<br><br>The procedure name is the place in the software where the error was detected. |
| Unable to get service/error log | An unsuccessful attempt was made to get a copy of the service or error log. |
| Unable to get calibration term | An unsuccessful attempt was made to get a calibration term. |
| Unable to get raw or corrected data | An unsuccessful attempt was made to get raw or corrected data. |
| Unable to get final data | An unsuccessful attempt was made to get final data. |
| Unable to get setup or data | An unsuccessful attempt was made to get the frequency list from the database. |
| Unable to get setup | An unsuccessful attempt was made to get a front panel setup. |

***Table B-3.*** *GPIB-Related Error Messages (8 of 8)*

| Error Message | Description |
|---|---|
| Unable to store setup | An unsuccessful attempt was made to save a front panel setup. |
| Unable to get frequency list | An unsuccessful attempt was made to get setup, trace, or tabular datat from the database. |
| Unable to store label | An unsuccessful attempt was made to store a label in the database. |
| Calibration step failure | An error occurred while waiting for completion of a data collection sequence in calibration. |

***Table B-4.*** *Service Log Error Messages (1 of 3)*

| | |
|---|---|
| 0000 INFORMATIONAL MESSAGE | 0511 A TO D COMM FAIL |
| 0000 SELF TEST INFO MESSAGE | 0512 A TO D 8 BIT D TO A FAIL |
| 0094 PRNT INTERFACE TEST PASSED | 0513 A TO D 12 BIT A TO D FAIL |
| 0095 PRNT INTERFACE TEST FAILED | 0514 A TO D STEERING DAC FAIL |
| 0096 GPIB INTERFACE TEST PASSED | 0515 A TO D CONV ACCURACY FAIL |
| 0097 GPIB INTERFACE TEST FAILED | 0516 A TO D SAMPL HOLD FAIL |
| 0098 SELF TEST PASSED | 0517 IF SYNC FAIL |
| 0099 SELF TEST FAILED | 0518 PWR SUPPLY SYNC FAIL |
| 0111 LO1 COMM FAIL | 0519 A TO D EXT ANAL OUTP FAIL |
| 0112 LO1 PRE TUNE DAC FAIL | 0520 PWR SUPPLY +5V FAIL |
| 0113 LO1 PHS LCK IND FAIL | 0521 PWR SUPPLY +9V FAIL |
| 0114 PHS LCK ERR VOL OUT OF TOL | 0522 PWR SUPPLY +12V FAIL |
| 0115 LO1 LCK TIME FAIL | 0524 PWR SUPPLY +18V FAIL |
| 0211 LO2 COMM FAIL | 0525 PWR SUPPLY -18V FAIL |
| 0212 LO2 MAIN PREST DAC FAIL | 0526 PWR SUPPLY +27V FAIL |
| 0213 LO2 OFFS PREST DAC FAIL | 0527 PWR SUPPLY -27V FAIL |
| 0214 MAIN PHS LCK ERR VOL FAIL | 0611 TB IF COMM FAIL |
| 0215 OFFST PHS LCK ERR VOL FAIL | 0612 TB IF 10V REF FAIL |
| 0216 DDS PHS LCK ERR VOL FAIL | 0613 TB IF LEVEL STATUS FAIL |
| 0217 MAIN PHS LCK IND FAIL | 0614 TB PHS CONTROL FAIL |
| 0218 OFFST PHS LCK IND FAIL | 0711 LO3 COMM FAIL |
| 0219 DDS PHS LCK IND FAIL | 0712 LO3 REF OSC FAIL |
| 0220 LO2 LCK TIME FAIL | 0713 LO3 48.4 LCK IND FAIL |
| 0221 LO2 SRC TRACKING FAIL | 0714 LO3 48.4 LCK ERR VOL FAIL |
| 0311 TA IF COMM FAIL | 0715 LO3 CAL REF PHS FAIL |
| 0312 TA IF 10V REF FAIL | 0811 SL SIG SEP COMM FAIL |
| 0313 TA IF LEVEL STATUS FAIL | 0812 DAC ADJUSTMENT FAIL |
| 0314 TA PHS CONTROL FAIL | 0813 TRANSFER SWITCH CNTRL FAIL |
| 0411 REF IF COMM FAIL | 0814 SRC LCK POL CONTROL FAIL |
| 0412 REF IF 10V REF FAIL | 0815 DIRECT MODE ATTEN FAIL |
| 0413 REF IF LEV STATUS FAIL | 0911 A9 VME BUS INTERFACE FAIL |
| 0414 REF PHS CONTROL FAIL | 0912 BBRAM CHECK FAIL |
| 0500 A TO D CONVERSION FAIL | 0913 SRAM CHECK FAIL |

***Table B-4.*** *Service Log Error Messages (2 of 3)*

| | |
|---|---|
| 0914 SCSI DEVICE FAIL | 2127 SRC ALC CAL BND1 FAIL |
| 0915 MCCHIP FAIL | 2128 SRC ALC CAL BND2 FAIL |
| 0915 MCCHIP TIMER 1 FAIL | 2129 SRC ALC CAL BND3 FAIL |
| 0916 MCCHIP TIMER 2 FAIL | 2130 SRC ALC CAL BND4 FAIL |
| 0917 MCCHIP TIMER 3 FAIL | 2131 SRC ALC CAL BND5 FAIL |
| 0918 MCCHIP TIMER 4 FAIL | 2132 SRC ALC CAL BND6 FAIL |
| 0919 CLOCK NOT RUNNING | 2133 SRC ALC CAL BND7 FAIL |
| 1311 A13 VME BUS INTERFACE FAIL | 2134 SRC ALC CAL BND8 FAIL |
| 1312 EXT KEYBD CNTRL FAIL | 2135 SRC ALC CAL BND9 FAIL |
| 1313 FLOPPY DISK CNTRL FAIL | 2136 SRC ALC CAL BND10 FAIL |
| 1411 A14 VME BUS INTERFACE FAIL | 2137 SRC A1 FM PATH TUNE FAIL |
| 1511 A15 VME BUS INTERFACE FAIL | 2138 SRC A2 FM PATH TUNE FAIL |
| 1512 VRAM CHECK FAIL | 4100 LO1 CAL FAIL |
| 1611 HARD DISK CONTROL FAIL | 4200 LO2 CAL FAIL |
| 1811 AUXILLARY IO FAIL | 4301 SRC FREQ CAL MEAS UNSTABLE |
| 1912 FRONT PANEL CNTRL FAIL | 4302 SRC FREQ FM MAIN CAL FAIL |
| 1913 ROTARY KNOB FAIL | 4303 SRC FREQ FM SENS CAL FAIL |
| 2111 SRC COMM FAIL | 4304 SRC FREQ CAL VERIFY FAIL |
| 2112 SRC FTUNE DAC FAIL | 4401 SRC ALC LOG AMP CAL FAIL |
| 2113 SRC STATE MACHINE DAC FAIL | 4402 SRC ALC CAL VERIFY FAIL |
| 2114 SRC FM CAL FAIL | 4500 IF CAL FAIL |
| 2115 SRC F TUNE PATH BND1 FAIL | 4600 GAIN RANGING ERROR |
| 2116 SRC F TUNE PATH BND2 FAIL | 4700 STATE MACHINE FAIL |
| 2117 SRC F TUNE PATH BND3 FAIL | 5110 RF PWR UNLEVELED |
| 2118 SRC F TUNE PATH BND4 FAIL | 5210 REF A CHAN RF OVERLOAD |
| 2119 SRC F TUNE PATH BND5 FAIL | 5220 REF B CHAN RF OVERLOAD |
| 2120 SRC F TUNE PATH BND6 FAIL | 5230 TA CHAN RF OVERLOAD |
| 2121 SRC F TUNE PATH BND7 FAIL | 5240 TB CHAN RF OVERLOAD |
| 2122 SRC F TUNE PATH BND8 FAIL | 6001 - 6128 PHASE LOCK FAILURE |
| 2123 SRC F TUNE PATH BND9 FAIL | 7100 FILE MARKED READ ONLY |
| 2124 SRC F TUNE PATH BND10 FAIL | 7140 GENERAL FLOPPY DRIVE FAIL |
| 2125 SRC PWR LEVEL DAC FAIL | 7142 FLOPPY DISK READ ERROR |
| 2126 SRC DETECTOR ZERO CAL FAIL | 7143 FLOPPY DISK WRITE ERROR |

***Table B-4.*** *Service Log Error Messages (3 of 3)*

| | |
|---|---|
| 7146 FLOPPY DISK CHANGED | 7222 PLOTTER OUT OF PAPER |
| 7147 FLOPPY DISK UNAVAILABLE | 7223 PLOTTER PEN UP |
| 7169 FLOPPY INIT FAIL | 7230 POWER METER NOT RESPONDING |
| 7170 GENERAL HARD DISK FAIL | 7240 FRQ COUNTER NOT RESPONDING |
| 7172 HARD DISK READ ERROR | 7250 EXT SOURCE NOT RESPONDING |
| 7173 HARD DISK WRITE ERROR | 7310 PRINTER NOT RESPONDING |
| 7177 HARD DISK UNAVAILABLE | 7311 PRINTER NOT READY |
| 7199 HARD DISK INIT FAIL | 7312 PRINTER OUT OF PAPER |
| 7200 IEEE 488.2 GPIB BUS ERROR | 7320 AUX I/O PORT ERROR |
| 7201 ABORTED MESSAGES | 7330 SERIAL PORT ERROR |
| 7202 NOTHING TO SAY | 7340 ETHERNET PORT ERROR |
| 7203 NO LISTENER ON BUS | 7350 EXT TRIG RATE TOO FAST |
| 7204 GPIB COMMAND ERROR | 7410 EXT KYBD ERROR |
| 7205 GPIB EXECUTION ERROR | 8100 PWR FAIL |
| 7206 GPIB DEVICE SPECIFIC ERROR | 8110 GENERAL VME BUS FAIL |
| 7207 GPIB QUERY ERROR | 8120 GENERAL MEMORY FAIL |
| 7210 DEDICATED GPIB BUS ERROR | 8121 NON-VOLATILE MEMORY FAIL |
| 7220 PLOTTER NOT RESPONDING | 8130 PROCESSING FAIL |
| 7221 PLOTTER NOT READY | 8140 GENERAL DISK BUFFER ERR |

# *Appendix C*
# *Connector Maintenance Check Procedures*

## *Table of Contents*


| | | |
|---|---|---|
| C-1 | INTRODUCTION | C-3 |
| C-2 | PRECAUTIONS | C-3 |
| | Pin Depth Problems | C-3 |
| | Pin-Depth Tolerance | C-4 |
| | Avoid Over Torquing Connectors | C-4 |
| | Teflon Tuning Washers | C-4 |
| | Avoid Mechanical Shock | C-4 |
| | Keep Connectors Clean | C-4 |
| | Visual Inspection | C-5 |
| C-3 | REPAIR/ MAINTENANCE | C-5 |

# *Appendix C*
# *Connector Maintenance Check Procedures*

## *C-1* INTRODUCTION

This appendix provides general, precautionary information and instructions pertaining to precision connectors.

## *C-2* PRECAUTIONS

The following paragraphs are precautionary notes relating to maintenance considerations for precision connectors

### *Pin Depth Problems*

Based on ANRITSU precision components returned for repair, destructive pin depth of mating connectors is the major cause of failure in the field. When a precision component is mated with a connector having a destructive pin depth, damage will likely occur to the precision component's connector. A connector is considered to have destructive pin depth when the center pin is too long in respect to the connector's reference plane (Figure C-1).

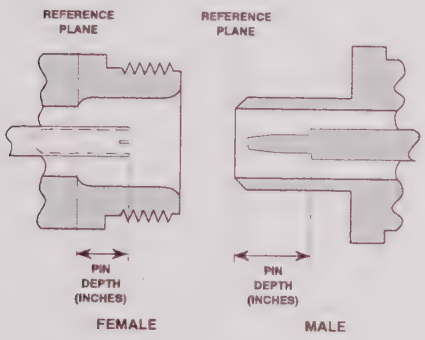



**Figure C-1.** *N Connector Pin Depth Definition*

Before mating an unknown or new device with your 373XXA Port connectors or calibration devices, always measure the pin depth of the device's connectors. Use a ANRITSU Pin Depth Gauge, or equivalent, for these measurements (Figure C-2). Also, measure the connector pin-depth of a device when intermittent or degraded performance is suspected.

Gauging sets for measuring the pin-depth of precision connectors are available from your nearest ANRITSU Service center, or from the factory. Instructions for measuring connector pin-depth are included with the gauging set(s).

**Figure C-2.** *Pin Depth Gauge*

***Pin-Depth Tolerance***

The center pin of a precision connector has a tolerances measured in mils (one mil = 1/1000 inch). The connectors of test devices may not be precision types and they may not have the proper pin-depth. These connectors should be measured before mating to ensure suitability.

When gauging pin depth, if the connector being measured indicates out of tolerance in the "+" region of the gauge (Table C-1), the center pin is too long. *Mating under this condition will likely damage the mating connector.* On the other hand, if the test device connector indicates out of tolerance in the "–" region, the center pin is too short. While this will not cause any damage, it will result in a poor connection and a consequent degradation in performance.

***Table C-1.*** *Connector Pin-Depth Tolerance*

| Port/ Conn. Type | Pin Depth (MILS) | Gauge Reading |
|---|---|---|
| GPC-7 | +0.000<br>–0.003 | Same As Pin Depth |
| N Male | 20 –0.000<br>7 +0.004 | 20 +0.000<br>7 –0.004 |
| N Female | 20 –0.004<br>7 +0.000 | Same As Pin Depth |
| 3.5 mm Male, Female | –0.000<br>+0.002 | |
| K Male, Female | +0.0000<br>–0.0035 | |
| V Male | +0.000<br>to –0.001 | |
| V Female | +0.000<br>to –0.001 | |

***Avoid Over Torquing Connectors***

Over-torquing connectors is destructive; it may damage the connector center pin. Finger-tight is usually sufficient, especially on Type N connectors. Should it be necessary to use a wrench to tighten SMA or WSMA connectors, use a torque wrench that breaks at 8 inch-pounds. As a general rule, *never use pliers to tighten connectors.*

***Teflon Tuning Washers***

The center conductor on many precision connectors contains a small teflon tuning washer located near the point of mating (interface). This washer compensates for minor impedance discontinuities at the interface. The washer's location is critical to the connector's performance. *Do not disturb it.*

***Avoid Mechanical Shock***

Precision connectors are designed to withstand years of normal bench handling. Do not drop or otherwise treat them roughly. They are laboratory-quality devices, and like other such devices, they require careful handling.

***Keep Connectors Clean***

The precise geometry that makes a precision connector's high performance possible can be disturbed by dirt and other contamination ad-

hering to connector interfaces. When not in use, keep the connectors covered.

***Visual Inspection***

Precision connectors should be inspected periodically. Check for the following:

- Bent or broken center pin
- Damaged threads
- Other bent or damaged connector parts
- Dirt or foreign material in connector cavity.

## C-3 REPAIR/ MAINTENANCE

ANRITSU recommends that no maintenance other than cleaning be attempted by the customer. Any device with a suspected defective connector should be returned to ANRITSU for repair and/or service when needed.

# *Appendix D*
# *Performance Specifications*

# Appendix D
# Performance Specifications

## SYSTEM PERFORMANCE

**Frequency Range:**

**RF Models:**

37317A 22.5 MHz to 8.6 GHz

**Microwave Models**

37325A 40 MHz to 13.5 GHz
37347A 40 MHz to 20 GHz
37369A 40 MHz to 40 GHz
37397A 40 MHz to 65 GHz

**Dynamic Range:**

The following table gives dynamic range in two manners. "Receiver Dynamic Range" is defined as the ratio of the maximum signal level at Port 2 for 0.1 dB compression to the noise floor at Port 2.

| Model | Freq (GHz) | Max Signal into Port 2 (dBm) | Noise Floor (dBm) | Receiver Dynamic Range | Port 1 Power (dBm) | System Dynamic Range |
|---|---|---|---|---|---|---|
| 37317A | 0.0225 | +30 | –95 | 125 | 0 | 95 |
| | 2 | +30 | –98 | 130 | 0 | 98 |
| | 8.6 | +30 | –98 | 130 | 0 | 98 |
| 37325A | 0.04 | +30 | –65 | 100 | +5 | 70 |
| | 2 | +30 | –93 | 128 | +5 | 98 |
| | 13.5 | +30 | –93 | 128 | +5 | 98 |
| 37347A | 0.04 | +30 | –65 | 100 | +5 | 70 |
| | 2 | +30 | –93 | 128 | +5 | 98 |
| | 20 | +30 | –91 | 126 | +5 | 96 |
| 37369A | 0.04 | +30 | –65 | 100 | +5 | 58 |
| | 2 | +30 | –93 | 128 | +5 | 86 |
| | 20 | +30 | –90 | 125 | 0 | 83 |
| | 40 | +30 | –83 | 123 | –7 | 76 |
| 37397A | 0.04 | +30 | –77 | 107 | +10 | 70 |
| | 2 | +30 | –105 | 135 | +10 | 98 |
| | 20 | +30 | –97 | 127 | –2 | 90 |
| | 40 | +30 | –95 | 125 | –7 | 88 |
| | 50 | +30 | –87 | 117 | –2 | 80 |
| | 65 | +30 | –77 | 107 | –2 | 70 |

"System Dynamic Range" is defined as the ratio of the power incident on Port 2 in a through line connection to the noise floor at Port 2 (forward measurements only). In preparing the table, 10 Hz IF bandwidth and 512 averages were used in calibration and measurement.

**High Level Noise (typical)**

<0.04 dB and <0.5° peak-to-peak variation in a 1 kHz IF bandwidth up to 20 GHz. <0.08 dB and <1.0° peak-to-peak variation up to 40 GHz. <0.25 dB and <2.5° peak-to-peak variation up to 65 GHz.

**Measurement Throughput:**

Measurement times are based on a single 40 MHz to 20 GHz sweep with 10 kHz IF bandwidth (no averages) after a full 12-term calibration. Sweep times include retrace and bandswitch times.

**Measurement Time (ms) vs. Data Points (typical):**

| Calibration Type | Data Points | | | | |
|---|---|---|---|---|---|
| | 3 | 51 | 101 | 401 | 1601 |
| 1 Port (3 Term) | 60 | 250 | 330 | 960 | 3300 |
| Full 2 Port | 60 | 270 | 400 | 1000 | 3600 |

**Measurement Time vs. Sweep Mode for 101 Data Points (typical):**

| Sweep Mode | Time (ms) |
|---|---|
| Linear | 350 |
| List | 350 |
| CW | 230 |

**Measurement Time vs. IF Bandwidth for 101 Data Points (typical):**

| IF Bandwidth | Time (ms) |
|---|---|
| 10 kHz | 350 |
| 1 kHz | 530 |
| 100 Hz | 1900 |
| 10 Hz | 14000 |

| Connector | Frequency (GHz) | Directivity (dB) | Source Match (dB) | Load Match (dB) | Reflection Frequency Tracking (dB) | Transmission Frequency Tracking (dB) | Isolation (dB) |
|---|---|---|---|---|---|---|---|
| GPC-7 | 0.0225 | >52 | >44 | >52 | ±0.003 | ±0.004 | >105 |
| | 2.0 | >52 | >44 | >52 | ±0.003 | ±0.004 | >115 |
| | 18 | >52 | >42 | >52 | ±0.004 | ±0.012 | >112 |
| GPC-7 LRL Calibration | 2.0 | >60 | >60 | >60 | ±0.001 | ±0.001 | >115 |
| | 18 | >60 | >60 | >60 | ±0.001 | ±0.001 | >112 |
| N-Type | 0.0225 | >46 | >36 | >46 | ±0.004 | ±0.004 | >105 |
| | 2.0 | >44 | >36 | >44 | ±0.004 | ±0.004 | >115 |
| | 18 | >40 | >32 | >40 | ±0.005 | ±0.012 | >112 |
| 3.5 mm | 0.0225 | >44 | >40 | >44 | ±0.005 | ±0.030 | >105 |
| | 2.0 | >44 | >40 | >44 | ±0.005 | ±0.030 | >115 |
| | 20 | >44 | >38 | >44 | ±0.006 | ±0.050 | >110 |
| | 26.5 | >44 | >34 | >44 | ±0.006 | ±0.070 | >102 |
| K | 0.0225 | >42 | >40 | >42 | ±0.005 | ±0.030 | >105 |
| | 2.0 | >42 | >40 | >42 | ±0.005 | ±0.050 | >115 |
| | 20 | >42 | >34 | >42 | ±0.006 | ±0.070 | >110 |
| | 40 | >38 | >34 | >38 | ±0.006 | ±0.080 | >100 |
| V | 0.04 | >70 | >36 | >40 | ±0.050 | ±0.030 | >105 |
| | 2.0 | >40 | >36 | >40 | ±0.050 | ±0.050 | >115 |
| | 20 | >40 | >36 | >40 | ±0.060 | ±0.070 | >110 |
| | 40 | >36 | >32 | >36 | ±0.060 | ±0.080 | >100 |
| | 50 | >34 | >30 | >34 | ±0.080 | ±0.100 | >90 |
| | 65 | >34 | >28 | >34 | ±0.100 | ±0.120 | >80 |

**Measurement Time vs. Span for 101 Data Points (typical):**

| Frequency Span | Time (ms) |
|---|---|
| 40 MHz to 40 GHz | 500 |
| 20 GHz to 40 GHz | 400 |
| 10 GHz to 11 GHz | 250 |

## TEST PORT CHARACTERISTICS

The specifications in the following table apply when the proper Model 34U Universal Test Port Adapters are connected, with or without phase equal insertables, to the test set ports and calibrated with the appropriate Anritsu or other designated calibration kit at 23°C ±3°C using the OSL calibration method with a sliding load to achieve 12-Term error correction (A 90 minute warm-up time is recommended.)

## MEASUREMENT CAPABILITIES

**Number of Channels:** Four independent measurement channels.

**Parameters:** S11, S21, S22, S12, or user-defined combinations of a1, a2, b1, and b2. All measurements are made without the need to manually reverse the test device.

**Measurement Frequency Range:** Frequency range of measurement can be narrowed within the calibration range without recalibration. CW mode permits single frequency measurements, also without recalibration. In addition, the system accepts N discrete frequency points where 2≤N≤1601.

**Domains:** Frequency Domain, CW Draw, and optional High Speed Time (Distance) Domain.

**Formats:** Log Magnitude, Phase, Log Magnitude and Phase, Smith Chart (impedance), Smith Chart (Admittance), Linear Polar, Log Polar, Group Delay, Linear Magnitude, Linear Magnitude and Phase, Real, Imaginary, Real and Imaginary, SWR, Power.

**Data Points:** 1601 maximum. Data points can be switched to a value of 801, 401, 201, 101, or 51 points without recalibration (if 1601 points were used in the calibration). In addition, the system accepts an arbitrary set of N discrete data points where: 2≤N≤1601. CW mode permits selection of a single data point without recalibration.

**Reference Delay:** Can be entered in time or in distance (when the dielectric constant is entered). Automatic reference delay feature adds the correct electrical length compensation at the push of a button. Software compensation for the electrical length difference between reference and test is always accurate and stable since measurement frequencies are always synthesized. In addition, the system compensates reference phase delay for dispersive transmission media, such as waveguide and microstrip.

**Markers:** Six independent markers can be used to read out measurement data. In delta-reference marker mode, any one marker can be selected as the reference for the

other five. Markers can be directed automatically to the minimum or maximum of a data trace.
**Enhanced Markers:** Marker search for a level or bandwidth, displaying an active marker for each channel, and discrete or continuous (interpolated) markers.
**Marker Sweep:** Sweeps upward in frequency between any two markers. Recalibration is not required during the marker sweep.
**Limit Lines:** Either single or segmented limit lines can be displayed. Two limit lines are available for each trace.
**Single Limit Readouts:** Interpolation algorithm determines the exact intersection frequencies of test data and limit lines.
**Segmented Limit Lines:** A total of 20 segments (10 upper and 10 lower) can be generated per data trace. Complete segmented traces can be offset in both frequency and amplitude.
**Test Limits:** Both single and segmented limits can be used for PASS/FAIL testing. The active channel's PASS or FAIL status is indicated on CRT after each sweep. In addition, PASS/FAIL status is output through the rear panel I/O connector as selectable TTL levels (PASS=0V, FAIL=+5V, or PASS=+5V, FAIL=0V).
**Tune Mode:** Tune Mode optimizes sweep speed in tuning applications by updating forward S-parameters more frequently than reverse ones. This mode allows the user to select the ratio of forward sweeps to reverse sweeps after a full 12-term calibration. The ratio of forward sweeps to reverse sweeps can be set anywhere between 1:1 to 10,000:1.

## DISPLAY CAPABILITIES

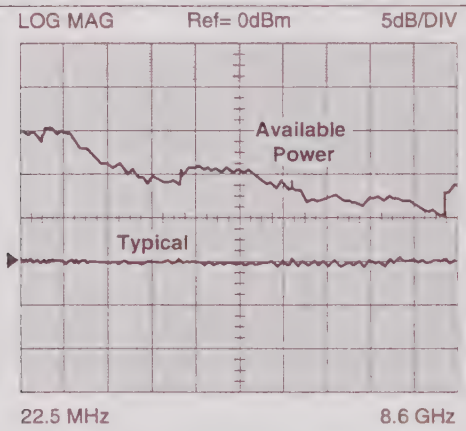
**Display Channels:** Four, each of which can display any S-parameter or user defined parameter in any format with up to two traces per channel for a maximum of eight traces simultaneously. A single channel, two channels (1 and 3, or 2 and 4), or all four channels can be displayed simultaneously. Channels 1 and 3, or channels 2 and 4 can be overlaid.
**LCD:** Color, 8.5-inch diagonal.
**Trace Color:** The color of display traces, memory, text, markers and limit lines are all user definable.
**Trace Overlay:** Displays two data traces on the active channel's graticule simultaneously. The overlaid trace is displayed in yellow and the primary trace is displayed in red.
**Trace Memory:** A separate memory for each channel can be used to store measurement data for later display or subtraction, addition, multiplication or division with current measurement data.
**Scale Resolution (minimum):**
**Log Magnitude:** 0.001 dB/div
**Linear Magnitude:** 1 pU
**Phase:** 0.01°
**Group Delay:** 0.001 ps
**Time:** 0.001 ms
**Distance:** 0.1 µm
**SWR:** 1 pU
**Power:** 0.05 dB
**Autoscale:** Automatically sets Resolution and Offset to fully display measurement data.
**Reference Position:** Can be set at any graticule line.
**Annotation:** Type of measurement, vertical and horizontal scale resolution, start/stop or center/span frequencies, and reference position.
**Blank Frequency Information:** Blanking function removes all references to displayed frequencies on the CRT. Frequency blanking can only be restored through a system reset or GPIB command.

## MEASUREMENT ENHANCEMENT

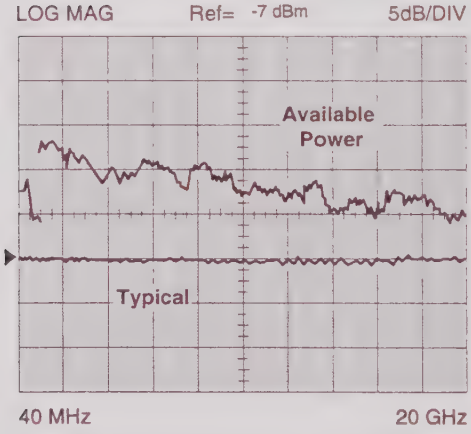
**Data Averaging:** Averaging of 1 to 4096 averages can be selected. Averaging can be toggled on/off with front panel button. A front panel button turns data averaging on/off, and a front panel LED indicates when averaging is active.
**Video IF Bandwidth:** Front panel button selects four levels of video IF bandwidth. MAXIMUM (10 kHz), NORMAL (1 kHz), REDUCED (100 Hz) and MINIMUM (10 Hz).
**Trace Smoothing:** Functions similarly to Data Averaging but computes an average over a percentage range of the data trace. The percentage of trace to be smoothed can be selected from 0 to 20% of trace. Front panel button turns smoothing on/off, and front panel LED indicates when smoothing is active.

## SOURCE CONTROL

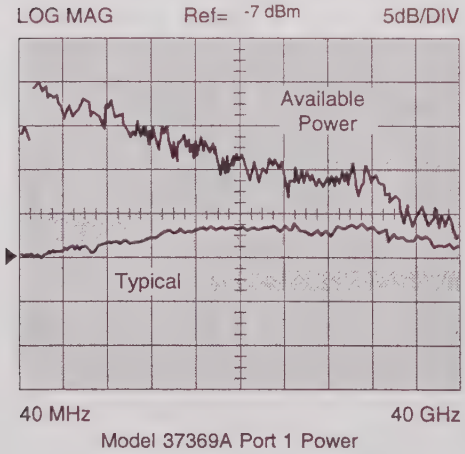
**Frequency Resolution:** 1 kHz (1 Hz standard on RF units and optional on Microwave units - Option 10A)
**Source Power Level:** The source power (dBm) may be set from the 373XXA front panel menu or via GPIB. Refer to Level Control Range table on next page.
In addition, the port 1 power may be attenuated in 10 dB steps, using the internal 70 dB (60 dB for 37397A) step attenuator. Similarly, high input signals into port 2, not exceeding 1 watt, can be attenuated up to 40 dB, using the internal port 2 step attenuator.
**Power Accuracy:** ±0.5 dB at 2 GHz at default power.
**Power Meter Correction:** The 373XXA offers a user-selectable feature that corrects for test port power variations and slope (on Port 1) using an external Hewlett-Packard 437B or Anritsu ML8403 power meter. Power meter correction is available at a user-selectable power level, if it is within the power adjustment range of the internal source. Once the test port power has been flattened, its level may be changed within the remaining power adjustment range of the signal source.
**Set-On Receiver Mode:** The 373XXA can be configured to measure the relative harmonic level of test devices with Set-On Receiver Mode capability. The 373XXA's unique



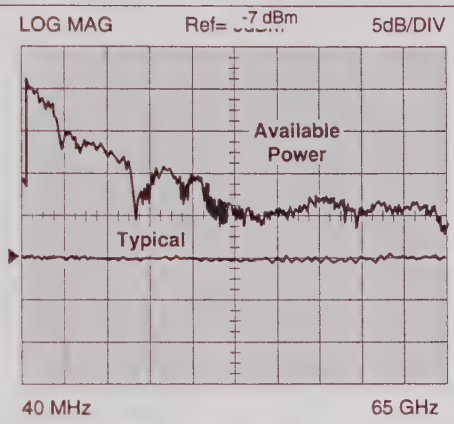

Model 37317A Port 1 Power




Model 37325A and 37347A Port 1 Power




Model 37369A Port 1 Power




Model 37397A Port 1 Power

phase locking scheme allows it to operate as a tuned receiver by locking all of its local oscillators to its internal crystal reference oscillator. Set-On Receiver Mode capability significantly increases the versatility of the 373XXA VNA in applications that check for harmonics, intermodulation products, and signals of known frequency.

**Dual Source Control Capability:** Dual Source Control capability allows a user to independently control the frequencies of two sources and the receiver without the need for an external controller. The frequency ranges and output powers of the two sources may be specified. A frequency sweep may be comprised of up to five separate bands, each with independent source and receiver settings, for convenient testing of frequency translation devices such as mixers. Up to five sub-bands may be tested in one sweep. This feature enables users to easily test mixers, up/down converters, multipliers, and other frequency conversion devices.

**Source 1:** The 373XXA internal source or any of the family of 68XXXB, 69XXXA, or 6700B synthesizers..

**Source #2:** Any of ANRITSU's family of 68XXXB, 69XXXA, or 6700B synthesizers.

**Sweep Type:** Linear, CW, Marker, or N-Discrete point sweep.

**POWER RANGE**

| Model | Rated Power (dbm) | Minimum Power (dBm) | Resolution (dB) |
|---|---|---|---|
| 37317A | 0 | –95 | 0.05 |
| 37325A | +5 | –90 | 0.05 |
| 37347A | +5 | –90 | 0.05 |
| 37369A | –7 | –97 | 0.05 |
| 37397A | –7 | –79 | 0.05 |

### LEVEL CONTROL RANGE
(Without step attenuator)

| | 37317A | 37325A | 37347A | 37369A | 37397A |
|---|---|---|---|---|---|
| Above Reset Power* | +10 dB | +10 dB | +10 dB | +20 dB | +20 dB |
| Below Reset Power | –25 dB | –25 dB | –25 dB | -20 dB | -20 dB <47 GHz<br>-12 dB ≥47 GHz |

*Source power above the reset level is allowed but not guaranteed, especially over the full frequency range.

### POWER FLATNESS

| Frequency Range (GHz) | Flatness (dB) |
|---|---|
| 0.0225 to 13.5 | ±1.5 |
| 13.5 to 20 | ±2.0 |
| 20 to 40 | ±3.0 |
| 40 to 65 | ±5.0 |

### SOURCE PURITY

***(Specifications apply for all models at maximum rated power.)***

**Harmonics & Harmonic Related:**
15 dBc (37325A, 37347A, 37369A, 37397A)
35 dBc (37317A)

**Nonharmonics:** 35 dBc (standard)
**Phase Noise:** >60 dBc/Hz at 10 kHz offset and 20 GHz center frequency

### SOURCE FREQUENCY ACCURACY

**Standard Time Base:**
**Aging:** $<1 \times 10^{-6}$/year
**Stability:** $<1 \times 10^{-6}$ over +15°C to +50°C range
**High Stability Time Base (Option 10):**
**Aging:** $<1 \times 10^{-9}$/day
**Stability:** $<5 \times 10^{-9}$ over 0°C to +55°C range

### GROUP DELAY CHARACTERISTICS

Group Delay is measured by computing the phase change in degrees across a frequency step by applying the formula:

$$\tau_g = -1/\frac{1}{360}\frac{d\Phi}{df}$$

**Aperture:** Defined as the frequency span over which the phase change is computed at a given frequency point. The aperture can be changed without recalibration. The minimum aperture is the frequency range divided by the number of points in calibration and can be increased to 20% of the frequency range without recalibration. The frequency width of the aperture and the percent of the frequency range are displayed automatically.

***Range:*** The maximum delay range is limited to measuring no more than +180° of phase change within the aperture set by the number of frequency points. A frequency step size of 100 kHz corresponds to 10 ms.

***Measurement Repeatability (sweep to sweep):*** For continuous measurement of a through connection, RSS fluctuations due to phase and FM noise are:

$$\frac{141\ [\,(\,Phase\ Noise\ \ in\ deg\,)^2\ +\ (\,\tau_g \times Residual\ FM\ Noise\ in\ Hz\,)^2\,]^{0.5}}{360\,(\,Aperture\ \ in\ \ Hz\,)}$$

**Accuracy:**

$$Error\ \ in\ \tau_g = \frac{\backslash\ Error\ in\ Phase\ (deg\,)}{360} + [\tau_g \times\ Aperture\ \ Freq.\ \ Error\ \ (Hz)\,]$$
$$Aperture\ (Hz)$$

### VECTOR ERROR CORRECTION

There are five methods of calibration:

**1) Open-Short-Load (OSL).** This calibration method uses short circuits, open circuits, and terminations (fixed or sliding)

**2) Offset-Short (waveguide):** This calibration method uses short circuits and terminations.

**3) LRL/LRM:** The Line-Reflect-Line (LRL) or Line-Reflect-Match (LRM) calibration uses transmission lines and a reflective device or termination (LRM).

**4) TRM:** The Thru-Reflect-Match calibration uses short circuits and fixed termination.

**5) AutoCal:** The VNA will serially drive an external AutoCal module to perform a 2-port OSLT calibration. AutoCal is a single two port calibration module with built-in, switched, and characterized OSLT standards. AutoCal provides quick, reliable, and accurate calibrations that exceed the performance of a standard broadband load OSLT calibration.

There are four vector error correction models available:

**1) Full 12-Term**
**2) One Path/Two Port**
**3) Frequency Response (Transmission/Reflection)**
**4) Reflection Only**

Full 12-term can always be used, if desired, since all 373XXA-series models automatically reverse the test signal. Front-panel display indicates the type of calibration stored in memory. Front-panel button selects whether calibration is to be applied, and an LED lights when error correction is being applied.

**Calibration Sequence:** Prompts the user to connect the appropriate calibration standard to Port 1 and/or Port 2. Calibration standards may be measured simultaneously or one at a time.

**Calibration Standards:** For coaxial calibrations the user selects SMA, GPC-3.5, GPC-7, Type N, 2.4 mm, TNC, K, or V Connector from a calibration menu. Use of fixed or sliding loads can be selected for each connector type. User defined calibration standards allow for entry of open

capacitance, load and short inductances, load impedance, and reflection standard offset lengths.
**Reference Impedance:** Modify the reference impedance of the measurement to other than 50 ohms (but not 0).
**LRL/LRM Calibration Capability:** The LRL calibration technique uses the characteristic impedance of a length of transmission line as the calibration standard. A full LRL calibration consists merely of two transmission line measurements, a high reflection measurement, and an isolation measurement. The LRM calibration technique is a variation of the LRL technique that utilizes a precision termination rather that a second length of transmission line. A third optional standard, either Line or Match, may be measured in order to extend the frequency range of the calibration. This extended calibration is achieved by mathematically concatenating either two LRL, two LRM, or one LRL and one LRM calibration(s). Using these techniques, full 12-term error correction can be performed on the 373XXA VNA.

**Adapter Removal Calibration:** Built-in Adapter Removal application software accurately characterizes and "removes" any adapter used during calibration what will not be used for subsequent device measurements. This technique allows for accurate measurement of non-insertable devices.
**Dispersion Compensation:** Selectable as Coaxial (non-dispersive), Waveguide, or Microstrip (dispersive).
**Reference Plane:** Selectable as Middle of line 1 or Ends of line 1.
**Corrected Impedance:** Determined by Calibration Standards.

### HARD COPY

**Printer:** Menu selects full screen, graphical, tabular data, S2P or Text output, and printer type. The number of data points of tabular data can be selected as well as data at markers only. Compatible with the 2225C InkJet, HP QuietJet, HP 310/320/340 DeskJet, HP 500 Deskjet, HP 560C DeskJet (b/w only), HP LaserJet II, III, & IV Series, and some Epson compatible printers with Parallel (Centronics) interfaces.
**GPIB Plotters:** The 37XXX VNA is compatible with HP Models 7440A, 7470A, 7475A, and 7550A (in standard mode) and Tektronix Model HC100 plotters. Menu selects plotting of full or user-selected portions of graphical data. Plotter is connected to the dedicated GPIB bus.
**Performance:** After selecting the Start Print button, front panel operation and measurement capability is restored to the user within 2 seconds.

### STORAGE

**Internal Memory:** Ten front panel states (setup/calibration) can be stored and recalled from non-volatile memory locations. The current front panel setup is automatically stored in non-volatile memory at instrument power-down. When power is applied, the instrument returns to its last front panel setup.
**Internal Hard Disk Drive:** Used to store and recall measurement and calibration data and front-panel setups. All files are MS-DOS compatable. File names can be 1 to 8 characters long, and must begin with a character, not a number. Extensions are automatically assigned.
**External SCSI Interface:** Option 4 deletes the internal hard disk drive, and adds a SCSI Interface connector to the rear panel for connecting a SCSI-2 formatted hard disk drive.
**Internal Floppy Disk Drive:** A 3.5-inch diskette drive with 1.44 Mbytes formatted capacity is used to load measurement programs and to store and recall measurement and calibration data and front panel setups. All files are MS-DOS compatable. File names can be 1 to 8 characters long, and must begin with a character, not a number. Extensions are automatically assigned.
**Measurement Data:** 102.8 kbytes per 1601 point S-parameter data file.
**Calibration Data:** 187.3 kbytes per 1601 point S-parameter data file (12-term cal plus setup).
**Trace Memory File:** 12.8 kbytes per 1601 point channel.

### GPIB

**GPIB INTERFACES - 2 PORTS**
**System GPIB (IEEE-488.2):** Connects to an external controller for use in remote programming of the network analyzer. Address can be set from the front panel and can range from 1 to 30.
**Interface Function Codes:** SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP1, DT1, DC0, C0.
**Dedicated GPIB:** Connects to external peripherals for network analyzer controlled operations (e.g. GPIB plotters, frequency counters, frequency synthesizers, and power meters).
**GPIB Data Transfer Formats:** ASCII, 32-bit floating point, or 64-bit floating point. 32-bit and 64-bit floating point data can be transferred with LSB or MSB first.

### GPIB DATA COLLECTION SUMMARY

This section summarizes typical data collection times for automated measurements using the 37XXX IEEE 488.2 GPIB bus. Throughput measurements for both tables were made as follows: start the timer, trigger a sweep, wait for a full sweep, transfer data across the GPIB and stop the timer. Data throughput times are shown separately for measurements made without calibration and with full two-port, 12-term calibration.
**Data Transfer Speed (with or without cal):** 150 kbytes/second
**Measurement conditions:** 40 MHz to 20 GHz sweep, single channel, log magnitude display, 10 kHz IF bandwidth, and output final data.

**Throughput Times (ms) without Correction (typical)**

| Data Format | 3 Points* | 101 Points | 401 Points | 1601 Points |
|---|---|---|---|---|
| 32 Bit | 230 | 650 | 1400 | 3600 |
| 64 Bit | 230 | 680 | 1450 | 4000 |
| ASCII | 235 | 800 | 1700 | 5000 |

**Throughput Times (ms) with Correction (typical)**

| Data Format | 3 Points* | 101 Points | 401 Points | 1601 Points |
|---|---|---|---|---|
| 32 Bit | 340 | 1200 | 2600 | 7800 |
| 64 Bit | 350 | 1200 | 2700 | 8300 |
| ASCII | 350 | 1280 | 3000 | 9300 |

* Frequencies taken at 2, 4, and 6 GHz

## GENERAL

**37300A Front Panel Connectors and Controls:**

**Keyboard Input:** An IBM-AT compatible keyboard can be connected to the front panel for navigating through front panel menus and disk directories, annotation of data files and display labels, printing displays and pausing instrument sweeps.

**Test Ports:** Universal/K, male, connectors are standard on all models except for 37397A, which has V Connector test ports as standard. For other configurations check Option 7. For additional configurations check Test Port Converters.

**Bias Inputs:** Port 1 and 2: 0.5 amps maximum through BNC connectors.

**Port 1 Amplifier Loop:** Access to insert an external amplifier, ahead of the port 1 coupler or bridge, to increase port 1 power output, up to +30 dBm (1 watt) maximum.

**37300A Rear Panel Connectors and Controls:**

**PRINTER OUT:** Centronics interface for an external printer.

**VGA OUT:** Provides VGA output of 373XXA video display.

**10 MHz REF IN:** Connects to external reference frequency standard, 10 MHz, +5 to –5 dBm, 50 ohms, BNC female.

**10 MHz REF OUT:** Connects to internal reference frequency standard, 10 MHz, 0 dBm, 50 ohms, BNC female.

**EXT ANALOG OUT:** –10V to +10V with 5 mV resolution, varying in proportion to user-selected data (e.g., frequency, amplitude). BNC female.

**EXT ANALOG IN:** ±50 volt input for displaying external signals on the CRT in Diagnostics mode. BNC female.

**LINE SELECTION:** Power supply automatically senses 100V, 120V, 220V or 240V lines.

**EXTERNAL TRIGGER:** External triggering for 373XXA measurement, ±1V trigger. 10 kohm input impedance. BNC female.

**REFERENCE EXTENSION:** Provides access to a1 and b1 samplers; K or V Connector, female.

**EXTERNAL SCSI:** Provides SCSI-2 connector for connection of an external SCSI hard disk drive (Opt. 4).

**EXTERNAL I/O:** 25-pin DSUB connector.

**EXTERNAL SCSI:** Provides SCSI-2 connector for connection of an external SCSI hard disk drive (Opt. 4).

**SERIAL:** Provides control for AutoCal module.

**LIMITS PASS/FAIL:** Selectable TTL levels (Pass=0V, Fail=+5V or Pass=+5V, Fail=0V. Additionally, 0 volts (all displayed channels pass) or +5V (any one of 4 displayed channels fail) output pass/fail status (1 line).

**EXTERNAL TRIGGER:** External triggering for 373XXA measurement, ±1V trigger. 10 kohm input impedance. BNC female.

**EXT ANALOG OUT:** –10V to +10V with 5 mV resolution, varying in proportion to user-selected data (e.g., frequency, amplitude). BNC female.

**Power Requirements:** 85-240V, 48-63 Hz, 540 VA maximum

**Dimensions:** 267H x 432W x 585D mm (10.5H x 17W x 23D in.)

**Weight:** 34 kg (75 lb) - Maximum amount specified for 2-man lift requirement.

## ENVIRONMENTAL

**Storage Temperature Range:** –40°C to +75°C

**Operating Temperature Range:** –0°C to +50°C

**Relative Humidity:** 5% to 95% at +40°C

**EMI:** Meets the emissions and immunity requirements of
EN55011/1991 Class A/CISPR-11 Class A
EN 50082-1/1993
IEC 801-2/1984 (4 kV CD, 8kV AD)
IEC 1000-4-3/1995 (3 V/m, 80-1000 MHz)
IEC 801-4/1988 (500V SL, 1000V PL)
IEC 1000-4-5/1995 (2 kV L-E, 1kV L-L)

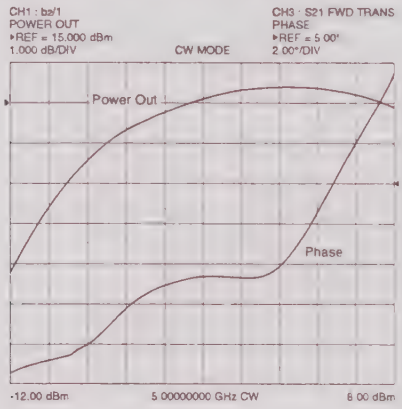
## GAIN COMPRESSION MEASUREMENT CAPABILITY

The 373XXA simplifies amplifier Gain Compression and AM/PM measurements. Once an appropriate power and frequency schedule is selected, a power meter calibration, at a set level, will calibrate the linear VNA receiver channels, to accurately measure power in dBm. The 37300A supports the HP437B, and Giga-tronics 8540B series power meters. To measure power, b2/1, a user defined parameter, is automatically selected.

**Swept Power Gain Compression:** The 373XXA will display traditional Power out vs. Power in or Phase vs. Power in, at one of up to 10 selectable frequencies. A separate screen will easily show Power out and Power in at 1 dB, or selected level Gain Compression, for all entered frequencies. (Check figure below).

**Swept Frequency Gain Compression:** Once Gain is measured at the starting power, the user increments Power in, observing Normalized Gain vs. Frequency. This aids in

analyzing the most critical compression frequencies of a broadband amplifier.




*Shows Power Out and Phase performance as a function of Input Power at a CW frequency.*

### HIGH SPEED TIME (DISTANCE) DOMAIN MEASUREMENT CAPABILITY (OPTION 2)

Option 2, High Speed Time (Distance) Domain software allows the conversion of reflection or transmission measurements from the frequency domain to the time domain. Measured S-parameter data is converted to the time domain by application of a Fast Fourier Transform (FFT) using the Chirp Z-Transform technique. Prior to conversion any one of several selectable windowing functions may be applied. Once the data is converted to the time domain, a gating function may be applied to select the data of interest. The processed data may then be displayed in the time domain with display start and stop times selected by the user or in the distance domain with display start and stop distance selected by the user. The data may also be converted back to the frequency domain with a time gate to view the frequency response of the gated data.

**Lowpass Mode:** This mode displays a response equivalent to the classic TDR (Time Domain Reflectometer) response of the device under test. Lowpass response may be displayed in either the impulse or step mode. This type of processing requires a sweep over a harmonic series of frequencies and an extrapolated or user-entered DC value.

**Bandpass Mode:** This mode displays a response equivalent to the time response of the device under test to a band limited impulse. This type of processing may be used with any arbitrary frequency sweep range, limited only by the test set range or device under test response.

**Phasor Impulse Mode:** This mode displays a response similar to the Lowpass impulse response, using data taken over an arbitrary (band limited) sweep range. Detailed information, similar to that contained in the lowpass impulse response may be used to identify the nature of impedance discontinuities in the device under test. Now, with Phasor Impulse, it is possible to characterize complex impedances on band-limited devices.

**Windowing:** Any one of four window functions may be applied to the initial frequency data, to counteract the effects of processing data with a finite bandwidth. These windows provide a range of tradeoffs of main lobe width versus sidelobe level (ringing).

The general type of function used is the Blackman-Harris window with the number of terms being varied from one to four. Typical performance follows:

| Types of Window (Number of Terms) | First Side Lobe Relative to Peak | Impulse Width[1] |
|---|---|---|
| Rectangular (1) | –13 dB | 1.2W |
| Nominal-Hamming (2) | –43 dB | 1.8W |
| Low Side Lobe, Blackman-Harris (3) | –67 dB | 2.1W |
| Minimum Side Lobe, Blackman-Harris (4) | –92 dB | 2.7W |

[1] W(Bin Width) = 1/2Δf sweep width
Example: When Δf = 40 MHz to 40 GHz, W = 12.5 ps
When Δf = 40 MHz to 65 GHz, W = 7.7 ps

**Gating:** A selective gating function may be applied to the time domain data to remove unwanted responses, either in a pass-band or reject-band (mask). This gating function may be chosen as the convolution of any of the above window types with a rectangular gate of user defined position and width. The gate may be specified by entering start and stop times or center and span. The gated data may be displayed in the time domain, or converted back to the frequency domain.

**Time Domain Display:** Data processed to time domain may be displayed as a function of time or as a function of distance, provided the dielectric constant of the transmission media is entered correctly. In the case of dispersive media such as waveguide or microstrip, the true distance to a discontinuity is displayed in the distance mode. The time display may be set to any arbitrary range by specifying either the start and stop times or the center time and span. The unaliased (non-repeating) time range is given by the formula:

$$UnaliasiedRange\ (ns) = \frac{Number\ of\ Frequency\ Data\ Points}{Frequency\ Sweep\ Range\ (GHz)}$$

The resolution is given by the formula:

$$Main\ Lobe\ Width\ (null \setminus null)\ in\ ns = \frac{kW}{Freq\ Sweep\ Range\ (GHz)}$$

Where kW is two times the number of window terms (for example, four for a two-term window)
For a 40 GHz sweep range with 1601 data points, the unaliased range is 40.025 nanoseconds.
For a 65 GHz sweep with 1601 data points, the unaliased range is 24.646 nanoseconds.
**Frequency with Time Gate:** Data that has been converted to time domain and selected by the application of gating function may be converted back to the frequency domain. This allows the display of the frequency response of a single element contained in the device under test. Frequency response accuracy is a function of window and gate type, and gate width. For a full reflection, minimum gate and window accuracy is within 0.2 dB of the ungated response over a 40 GHz range.

### MEASUREMENT UNCERTAINTY

The graphs on pages D-13 through D-15 give measurement accuracy after 12-term vector error correction. The errors are worst case contributions of residual directivity, load and source match, frequency response, isolation, network analyzer dynamic accuracy, and connector repeatability. In preparing the following graphs, 10 Hz IF bandwidth and averaging of 512 points were used (measured at 23±3° C). Changes in the IF bandwidth or averaging can result in variations at low levels.

### SYSTEM OPTIONS

**OPTION 1, Rack Mounting:** Rack mount kit containing a set of track slides (90 tilt capability), mounting ears, and front panel handles to let the instrument be mounted in a standard 19-inch equipment rack.
**OPTION 1A, Rack Mounting:** Rack mounting kit containing a set of mounting ears and hardware to permanently mount instrument in a standard 19-inch equipment rack.
**OPTION 2, High Speed Time (Distance) Domain Measurement Capability**
**OPTION 4, External SCSI-2 Hard Disk Drive Compatibility:** Provides SCSI-2 rear panel connector for connection of an external SCSI HDD. Remove internal HDD.
**OPTION 7A/N/NF/S/K, Universal Test Port Configuration Replaces Universal/K Connector (standard) with:**

- **7A -** Universal/GPC-7
- **7N -** Universal/N, male
- **7NF -** Universal/N, female
- **7S -** Universal/3.5 mm, male

**OPTION 10A, High Stability Time Base:** Replaces the standard temperature compensated crystal oscillator (with a temperature stability of 1ppm over a 0 to 55 °C range)with an ovenized crystal oscillator (aging stability of 1 x $10^{-9}$/day and temperature stability 5 x $10^{-9}$ over 0 to 55 °C range). Adds 1 Hz frequency resolution.

### UPGRADE OPTIONS*

**37200A** Upgrade to a higher frequency 37200A.
**37200A** Upgrade to an equivalent or higher frequency 37300A.
**37200B** Upgrade to a higher frequency 37200B.
**37200B** Upgrade to an equivalent or higher frequency 37300A.
**37300A** Upgrade to a higher frequency 37300A.

Please call your Anritsu representatives for pricing and delivery.

### ON-SITE SUPPORT

**Option ES 31:** 3 year on-site repair.
**Option ES 37:** 3 year on-site verification
**Option ES 38:** 3 year on-site Mil-Std verification
**Option ES 51:** 5 year on-site repair.
**Extended Service Options** Additional, two year and four year return to Anritsu service is available, as an option for 373XXA systems and components. Prices and details are available from your Sales Representative or by contacting the factory.

### CALIBRATION KITS

**Standard**
**3650 SMA/3.5 mm Calibration Kit**
**Option 1:** Male and Female Sliding Terminations
**3651 GPC-7 Calibration Kit**
**Option 1:** Sliding Terminations
**3652 K Connector Calibration Kit**
**Option 1:** Male and Female Sliding Terminations
**3653 Type N Calibration Kit**
**3654B Type V Calibration Kit;** includes male & female sliding terminations
**Economy (8.6 GHz)**
**3750 SMA Calibration Kit**
**3751 GPC-7 Calibration Kit**
**3753 Type N, 50 W, Calibration Kit**
**3753-75 Type N, 75 , Calibration Kit**

### VERIFICATION KITS

**3663 Type N Verifications Kit**
**3666 3.5 mm Verifications Kit**
**3667 GPC–7 Verifications Kit**
**3668 K Connector Verifications Kit**
**3669B V Connector Verifications Kit**

### SEMI-RIGID TEST PORT CABLES

**3670A50-1,** DC to 18 GHz, GPC–7 connectors, 1 foot long, two required.
**3670A50-2,** DC to 18 GHz, GPC–7 connectors, 2 feet long.
**3670K50-1,** DC to 40 GHz, K connectors, 1 foot long, male/female, two required.
**3670K50-2,** DC to 40 GHz, K connectors, 2 feet long, male/female.

**3670V50-1,** DC to 65 GHz, V connectors, 1 foot long, male/female, two required.
**3670V50-2,** DC to 65 GHz, V connectors, 2 feet long, male/female.

### FLEXIBLE TEST PORT CABLES

**3671A50-1 GPC-7 Flexible Cables,** 25 in. (1 pair).
**3671A50-2 GPC-7 Flexible Cable,** 38 in.
**3671S50-1 3.5mm Flexible Cables,** 25 in. (1 pair), male/male.
**3671S50-2 3.5mm Flexible Cable,** 38 in., male.
**3671K50-1 K Connector Flexible Cables,** 25 in. (1 pair), male/male.
**3671K50-2 K Connector Flexible Cable,** 38 in., male.
**3671V50-1 Universal Test Port Converter On Each Side,** moving the VNAs V-type test port converter to the end of the cable, 25 in., 2 each.
**3671V50-2 Universal Test Port Converter On Each Side,** moving the VNAs V-type test port converter to the end of the cable, 38 in., 1 each.
**NOTE:** All 3671-Series flexible test port cables mate to the standard 34UK50 Universal K Connector Test Port.

### TEST PORT CONVERTERS

**34UA50 Test Port Converter,** Universal/GPC-7
**34UK50 Test Port Converter,** Universal/K Connector, male
**34UN50 Test Port Converter,** Universal/N, male
**34UNF50 Test Port Converter,** Universal/N, female
**34UQ50 Test Port Converter,** Universal/2.4 mm, male
**34US50 Test Port Converter,** Universal/3.5 mm. male
**01-202,** Wrench, for changing test set Test Port Converters.

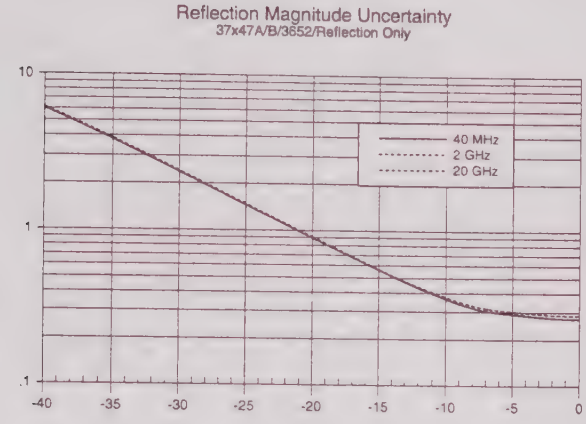
### GPIB CABLES

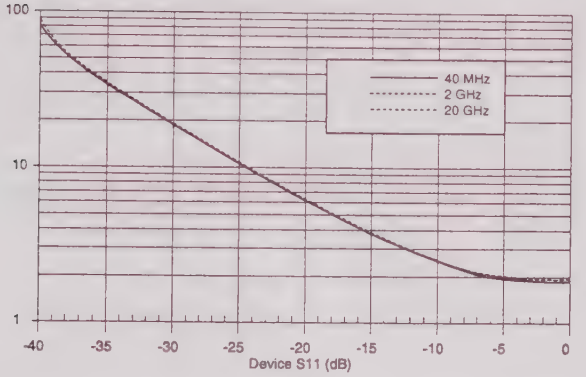
**2100-1 GPIB Cable,** 1 m (3.3 ft.)
**2100-2 GPIB Cable,** 2 m (6.6 ft.)
**2100-4 GPIB Cable,** 4 m (13.2 ft.)
**2100-5 GPIB Cable,** 0.5 m (1.65 ft.)

### ACCESSORIES

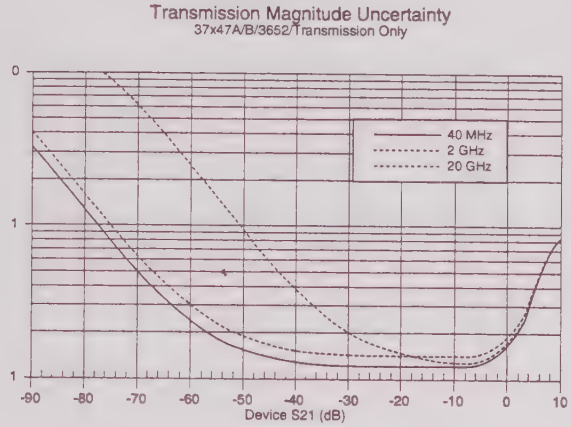
**2000-660 HP 310 Deskjet Printer,** Printer Stand, Deskjet Printer Cartridge and Power cord.
**2000-661 Extra Printer Cartridge**
**2000-662 Rechargeable Battery**
**2000-663 Power Cable,** Europe
**2000-664 Power Cable,** Australia
**2000-665 Power Cable,** U.K.
**2000-666 Power Cable,** Japan
**2000-667 Power Cable,** South Africa
**2225-1 Spare Parallel Interface Printer Cable**

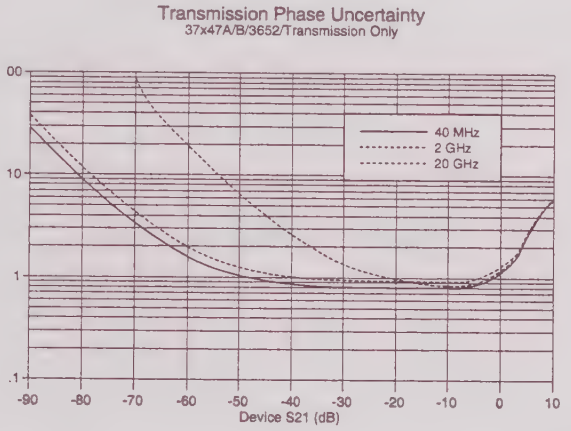
*Model 37347A (K Connectors)*
*Reflection Measurements:*



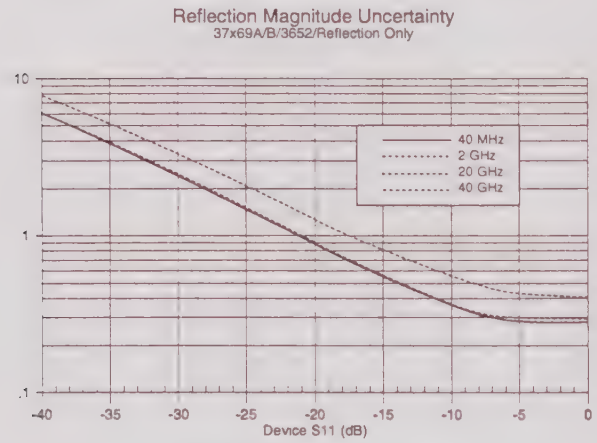



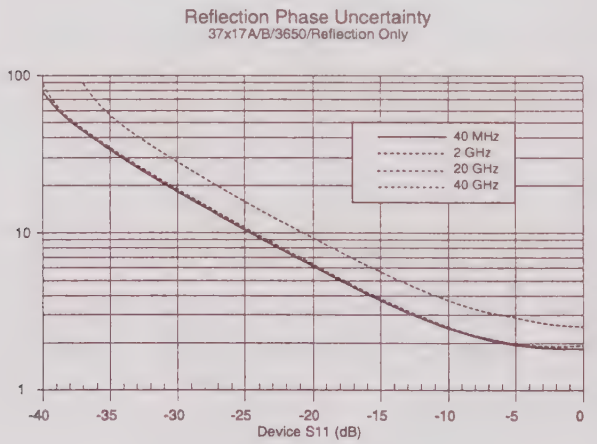

*Model 37347A (K Connectors)*
*Transmission Measurements:*



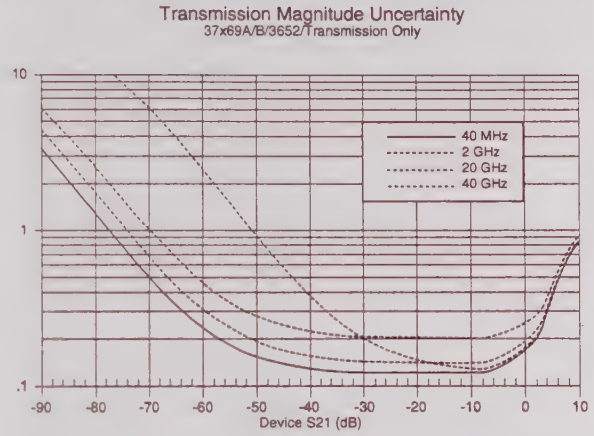



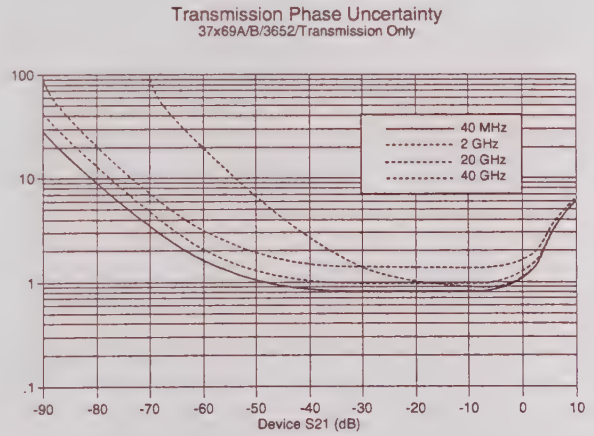
*Model 37369A (K Connectors)*
*Reflection Measurements:*



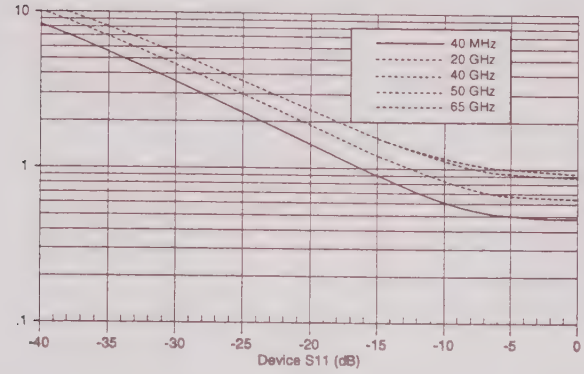

*Model 37369A (K Connectors)*
*Transmission Measurements:*



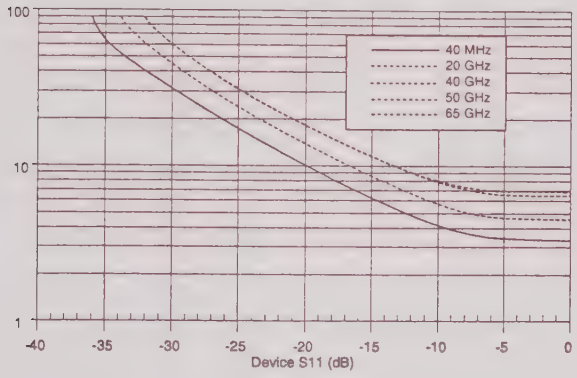



*Model 37397A (V Connectors)*
*Reflection Measurements:*

Reflection Magnitude Uncertainty
37x97A/B/3654B/Reflection Only

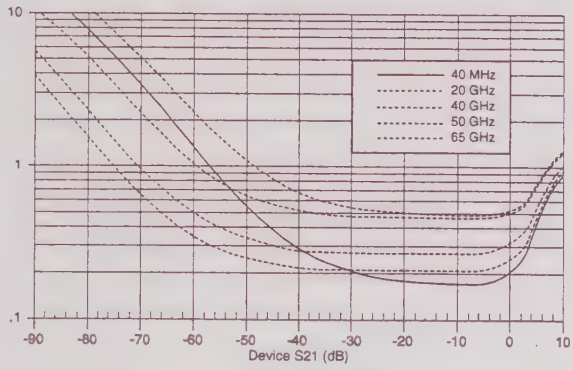



Reflection Phase Uncertainty
37x97A/B/3654B/Reflection Only

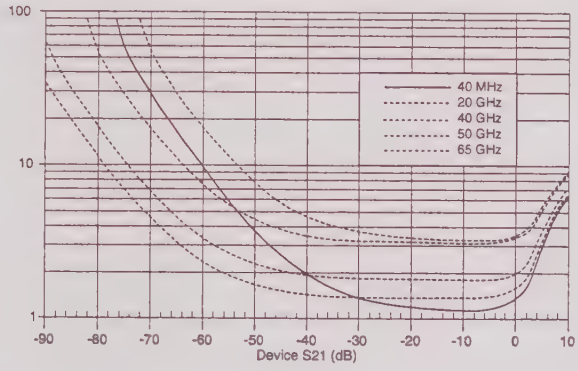



*Model 37397A (V Connectors)*
*Transmission Measurements:*

Transmission Magnitude Uncertainty
37x97A/B/3654B/Transmission Only




Transmission Phase Uncertainty
37x97A/B/3654B/Transmission Only



# *Appendix E*
# *Performance Verification Software User's Guide*

***This appendix contains the Model 360X/37XXX Vector Network Analyzer Performance VerificationSoftware User's Guide. This user's guide provides technical data and procedures that can aid you in performing maintenance on the 373XXA.***

# ANRITSU 2300-237
# Vector Network Analyzer
# Performance Verification

# *Software User's Guide*

***Software Revision 4.51***

Anritsu

490 JARVIS DRIVE
MORGAN HILL, CA 95037-2809

P/N: 10410-00208
REVISION: K
PRINTED: OCTOBER 2002
COPYRIGHT 2002 ANRITSU CO.

## LIMITED WARRANTY

The media on which you receive Anritsu Company software is warranted not to fail to execute programming instructions due to defects in materials and workmanship for a period of 90 days from date of shipment, as evidenced by receipts or other documentation. Anritsu Company will, at its option, repair or replace software media that does not execute programming instructions if Anritsu Company receives notice of such defects during the warranty period. Anritsu Company does not warrant that the operation of the software shall be uninterrupted or error free.

EXCEPT AS SPECIFIED HEREIN, ANRITSU COMPANY MAKE NO WARRANTIES, EXPRESS OR IMPLIED, AND SPECIFICALLY DISCLAIMS ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. CUSTOMER'S RIGHT TO RECOVER DAMAGES CAUSED BY FAULT OR NEGLIGENCE ON THE PART OF ANRITSU COMPANY SHALL BE LIMITED TO THE AMOUNT THERETOFORE PAID BY THE CUSTOMER. ANRITSU COMPANY WILL NOT BE LIABLE FOR DAMAGES RESULTING FROM LOSS OF DATA, PROFITS, USE OF PRODUCTS, OR INCIDENTAL OR CONSEQUENTIAL DAMAGES, EVEN IF ADVISED OF THE POSSIBILITY THEREOF.

The afore stated limitation of the liability of Anritsu Company will apply regardless of the form or action, whether in contract or tort, including negligence. Any action against Anritsu Company must be brought within one year after the cause of action accrues. Anritsu Company shall not be liable for any delay in performance due to causes beyond its reasonable control.

## TRADEMARK ACKNOWLEDGMENT

V Connector and K Connector are registered trademarks of Anritsu Company.
Pentium is a registered trademark of Intel Corp.
Windows is a registered trademark of Microsoft Corp.

## NOTICE

Anritsu Company has prepared this manual for use by Anritsu Company personnel and customers as a guide for the proper installation, operation and maintenance of Anritsu Company equipment and computer programs. The drawings, specifications, and information contained herein are the property of Anritsu Company, and any unauthorized use or disclosure of these drawings, specifications, and information is prohibited; they shall not be reproduced, copied, or used in whole or in part as the basis for manufacture or sale of the equipment or software programs without the prior written consent of Anritsu Company.

## CONTENTS


| | | Page |
|---|---|---|
| *Chapter 1* | *General Information* | *1* |
| *Chapter 2* | *Required Equipment* | *3* |
| *Chapter 3* | *Configuring the System* | *5* |
| *Chapter 4* | *Configuring the Program* | *7* |
| *Chapter 5* | *Running the Program* | *17* |
| *Chapter 6* | *Troubleshooting* | *23* |
| *Appendix A* | *Example of Tabular Test Results* | *25* |
| *Appendix B* | *GPIB Card and Instrument Settings* | *27* |
| *Appendix C* | *Instrument - Calibration Kit - Verification Kit Combinations* | *29* |

# Chapter 1
# General Information

Contents


| Paragraph | | Page |
|---|---|---|
| 1 | Introduction | 1 |
| 2 | Format of the Verification Software Disks | 1 |
| 3 | Capability | 1 |
| 4 | Data Output | 2 |


## 1 Introduction

This manual supports the Anritsu B52109 VNA Performance Verification Software. This software is used with the Anritsu Vector Network Analyzers and Vector Network Measurement Systems. The manual is organized into six chapters and three appendices, as shown below.

- *General Information*—Provides an overview of the product
- *Required Equipment*—Describes the test equipment, components, hardware and software required to use this product
- *Configuring the System*—Describes how the equipment is setup and interconnected
- *Configuring the Program*—Describes how to setup the software
- *Running the Program*—Provides step-by-step instructions for running the software
- *Troubleshooting*—Contains troubleshooting suggestions and service information
- *Appendix A*—Contains an example of tabular test results
- *Appendix B*—Provides GPIB card and instrument settings
- *Appendix C*—Lists instrument, calibration kit, and verification kit combinations

## 2 Format of the Verification Software Media

The Performance Verification Software is offered on IBM compatible CD-ROMs.

## 3 Capability

This software provides for automating measurements of the test components contained in an Anritsu Verification Kit.

It compares the measurements made on your VNA with the test component data provided in each verification kit. This will aid in determining if the measurement values are consistent with system specifications.

4

## Data Output

The test data and results are output in the form of four files to a directory (X:\installed directory) on your computers hard drive. The default file names, depending on the type of test being performed, are:

- 20db.dat
- 40db.dat or 50db.dat
- airline.dat
- beatty.dat

*NOTE*

This Performance Verification Software allows you to rename these files using the default ".dat" extension.

The tabular data in each file is given at discrete frequencies at 1.0 GHz intervals, along with separate start and stop frequencies if the start and stop frequencies do not fall on a 1 GHz spacing.

The test results can be viewed or printed from the "Main Menu" window.

# Chapter 2
# Required Equipment

Contents


| Paragraph | | Page |
|---|---|---|
| 5 | Introduction | 3 |
| 6 | Computer (System Controller) | 3 |
| 7 | GPIB Interface Card | 3 |
| 8 | Vector Network Analyzer | 4 |
| 9 | Verification Kit | 4 |
| 10 | Printer | 4 |
| 11 | Cables | 4 |


## 5 Introduction

This section describes the equipment required to use the performance verification software.

## 6 Computer (System Controller)

### Operating System

This software can be used with the following operating systems (U.S. English):

Microsoft Windows 95

Microsoft Windows NT 4.0

***NOTE***

This program may not function on international versions of Microsoft Windows that use double byte character sets.

### Hardware

IBM-compatible computer with 486 or faster microprocessor with a math coprocessor.

## 7 GPIB Interface Card

Depending upon the operating system and hardware used to perform the verification, there are different requirements for possible GPIB hardware configurations. This program has been tested with the following configurations:

Win95: National Instruments PCMCIA for Windows 95, Versions 1.2, 1.3, 1.4, 1.5 and 1.6

WinNT: GPIB Software for Windows NT (Intel) (NI-488.2M Software) Version 1.2, 1.3, 1.4, 1.5, and 1.6

Regardless of which GPIB hardware and software is used, the GPIB card must be configured as "GPIB0."

8

### Vector Network Analyzer

You need an Anritsu model 360X/37XXX(A/B/C) Vector Network Analyzer System, with the appropriate 3650, 3651, 3652, 3653, 3654, 3654B, 36581NNF, 36581KKF or 36582KKF calibration kit. A 360X system consists of a 360/360A/360B VNA, a 36XX-series test set, and an Anritsu RF signal source. Refer to Appendix B if this software is to be used with a 360X system. The 360X/37XXX(A/B/C) Vector Network Analyzer may be referred to as VNA throughout this Software User's Guide.

9

### Verification Kit

You need an Anritsu 3663, 3666, 3667, 3668, 3669, or 3669B verification kit with a Version 2 data disk.

*NOTE*

This program will not work with a "Version 1" verification kit data disk.

10

### Printer

A printer is not required for operation as the verification results and data are stored in four files on the computer hard disk drive. These files are saved in ASCII format for easy viewing and printing.

11

### Cables

You need a GPIB cable (Anritsu PN: 2100-2) and a two-foot RF test port cable (Anritsu PN: 3670A50-2, 3670K50-2, 3670V50-2, 3671A50-2, 3671K50-2, or 3671V50-2). If a verification of an AutoCal calibration is to be performed, refer to the AutoCal's product documentation that was supplied with the unit for a list of cable requirements.

*NOTE*

The Anritsu AutoCal product is not compatible with 360, 360A, or 37100A VNAs. Therefore, the verification program will not work in these instances. The Anritsu AutoCal product is compatible for use with Anritsu 360B, 372XX(A/C), or 373XXA series VNAs.

# Chapter 3
# Configuring the System

Contents


| Paragraph | | Page |
|---|---|---|
| 12 | Introduction | 5 |
| 13 | Hardware Interconnection | 5 |
| 14 | PV Software Installation and Configuration | 6 |
| 15 | AutoCal Installation and Configuration | 6 |


12

## Introduction

This chapter describes how the various system elements are interconnected and the preliminary steps required for operation of the verification software.

13

## Hardware Interconnection

Connect the computer's GPIB port to the VNA system using the GPIB cable.

If the VNA is a 360X network analyzer, connect to the GPIB connector labeled "360 GPIB" ***not*** the one labeled "System Bus."

If the VNA is a 37XXXX network analyzer, connect to the GPIB connector labeled "IEEE 488.2 GPIB" ***not*** the one labeled "Dedicated GPIB."

Connect the two-foot test port cable female end to the VNA Port 2.

Connect a female-female phase equal insertable adapter from the calibration kit to the VNA Port 1. This does not apply to GPC-7 calibrations.

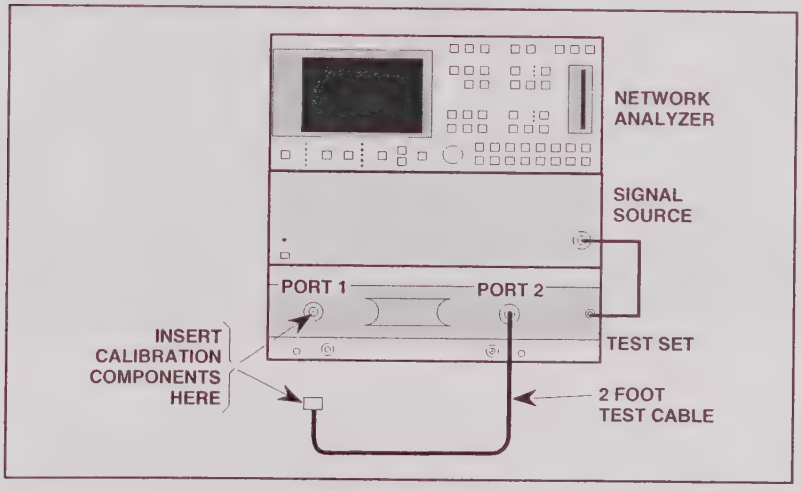



**Figure 1.** VNA Calibration and Measurement Setup Shown on a 360X VNA

14

## Performance Verification (PV) Software Installation

### CD ROM

Insert the CD-ROM into your CD-ROM drive. The installation program should run automatically. Follow the instructions on the screen. If the installation program does not start automatically then using *Windows Explorer* or the *My Computer* icon browse to the root directory of the CD-ROM. Double click the *Startup.exe* program to begin the installation process.

### Floppy Disk

The program installation files, *Setup.exe, Setup.W02,* etc., in the CD-ROM's program directory can be copied to floppy disks for installation on PC's without CD-ROM drives. Each *Setup.** file will need to be on its own floppy disk. Label the first "Disk 1," the second "'Disk 2," etc.

Put the disk labeled "VNA Verification Setup Disk 1" into the 3.5-inch high-density-floppy drive. From the Task Bar [TB], select the Start—Run command sequence and type `X:\setup.exe`, where `X` is the drive letter of the floppy drive the disk is in. Press the Enter key.

The setup program will copy the files to your PC into the directory of your choice (you will be prompted for the destination directory). Unlike previous versions, this program cannot be run from a floppy disk directly. When the setup program is completed, the program may or may not want to restart Windows, depending if there were any files in use (usually DLLs) at the time of the installation.

***NOTE***

Refer to Appendix B if this software is to be used with a 360X system.

15

## AutoCal Hardware/Software Installation

Follow the instructions in the AutoCal manual for these procedures. Refer to Figure 1 when connecting an AutoCal module to the VNA for an AutoCal calibration.

If an Anritsu 36581NNF or a 36582KKF AutoCal module (known as calibration components) are to be used, there are some special considerations that must be made in order to successfully pass the verification. These are discussed later in the "Running the Program" section. The program will also advise you of these considerations at the proper time.

# Chapter 4
# Configuring the Program

Contents


| Paragraph | | Page |
|---|---|---|
| 16 | Introduction | 7 |
| 17 | Starting the Program | 7 |
| 18 | Program Initialization | 8 |


16

## Introduction

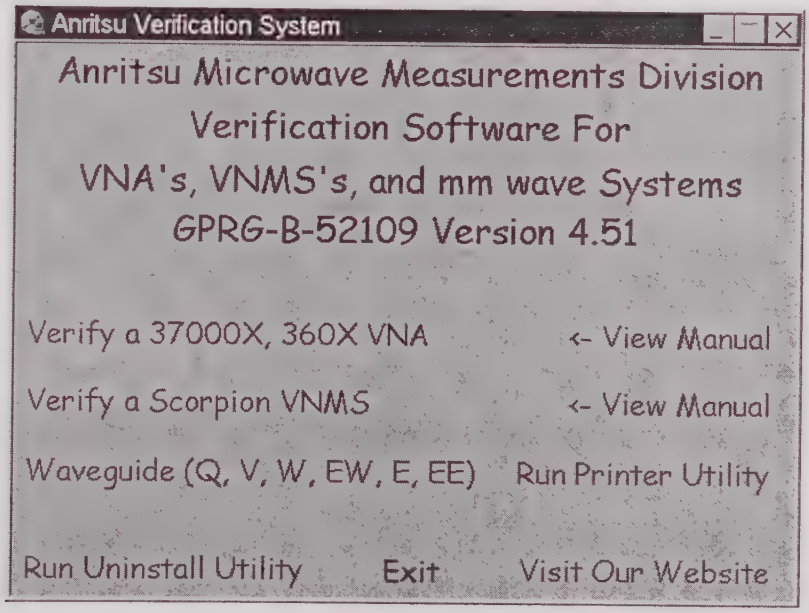
This performance verification software runs in a Windows environment as described below.

17

## Starting the Program

With the equipment and software configured as described in Chapter 3, turn on the computer and allow it to boot up to Windows.

Locate the verification software icon on the desktop and double-click on it. The program launcher menu will be displayed (as shown below).




At this point you can install the 3.5-inch data disk from the verification kit into an available floppy drive.

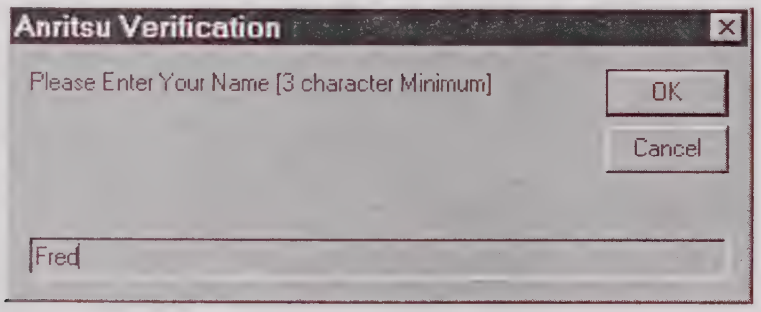
The program will display an animated Splash screen.

The program will display an About dialog box with version information. Press OK or Enter to continue.

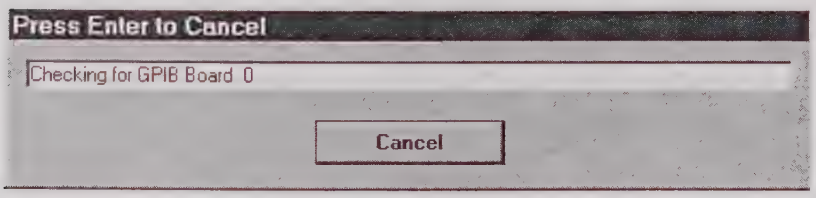
18

**Program Initialization**

You will be prompted to enter your name.

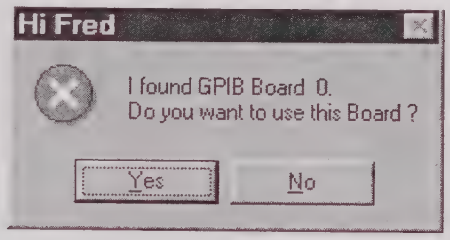



After you enter your name, the program will check for a GPIB card at the location GPIB0.

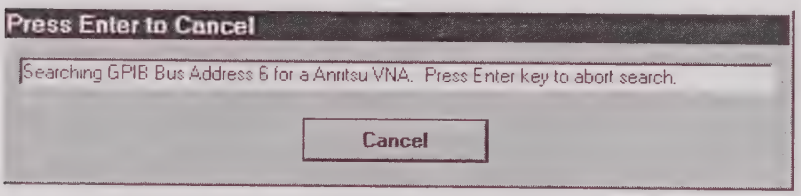



If the program finds a GPIB board at GPIB0 the program will continue. If the program does not find a GPIB Board at GPIB0, or if you answer No to the Dialog Box below, the program will terminate.

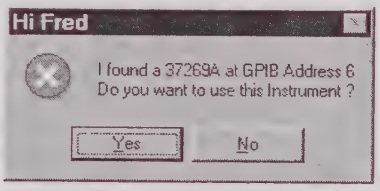
At this point you should answer Yes to this question.

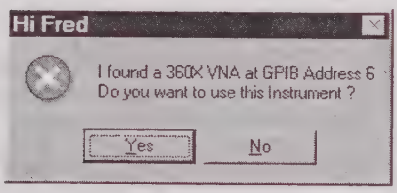



Next, the program will search the GPIB bus for an Anritsu VNA. If the program finds an Anritsu VNA, the program will respond differently depending upon the VNA type (360X or 37000 series) that is connected to the GPIB Bus.

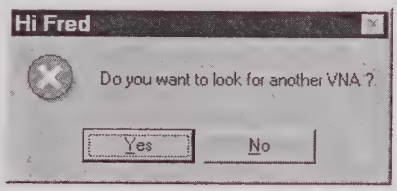



If the program finds a VNA, it will ask you for information about the VNA you want to use for the verification.




If there are multiple VNA's on the GPIB Bus, and this VNA is not the one you want to verify, then you should answer No so the program will look for another VNA on the GPIB Bus.



If you answer Yes to any of the previous dialogs, the program will respond differently depending on which family the VNA belongs to (37000 or 360X). If the program found a 360 series VNA, it will ask you several questions to gather information about the setup that cannot be determined by the program.

First the program prompts for the VNA model number:

- Is the VNA a '360B' Model?
  There is a 360B on the front panel. (Yes or No)
- Is the VNA a '360A' Model?
  Serial Numbers 808XXX thru 032XXX.
  Some VNA's in the 033XX series. (Yes or No)
- Is the VNA a '360 Non A'?
  Serial Number 807XXX or earlier. (Yes or No)

then prompts for:

- The VNA Serial Number (minimum 5 characters)
- The Source Model Number (minimum 4 characters)
- The Source Serial Number (minimum 5 characters)
- The Test Set Serial Number (minimum 5 characters)

Since most of the prior information does not pertain to a 37000 series VNA, the program will not ask those questions when a 37000 series is found. The information the program needs for a 37000 Series VNA is obtained from the instrument itself.

If the program did not find a VNA on the GPIB Bus, the program will tell you that it did not find one, then exit. If there is indeed a VNA on the GPIB Bus and the program did not find it, then there is a problem somewhere in the system. Check the cables to make sure they are properly connected and check the GPIB system to verify that it is operating properly. If this does not alleviate the problem, there could be something wrong with the GPIB system on the VNA.

In this section of the program, items that are determined by the program to be complete enough to continue to the next step will have the Frames Text Label change color from red to green to give you an indication to proceed.

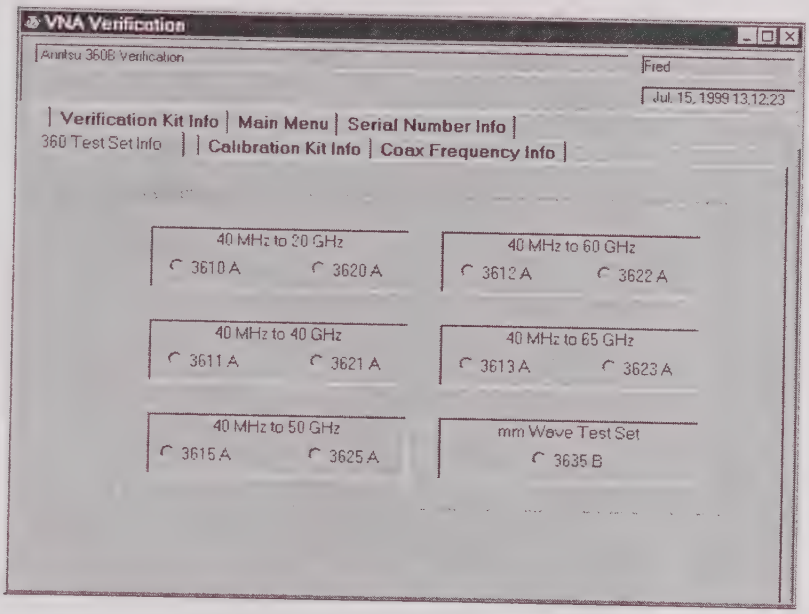
If the next item is a text box that needs to be filled in, the program will automatically move the cursor to that text box.

If the next item is a multiple choice item, the program will enable the choice's frame box and turn the label of the box red to draw the Operators attention to it.

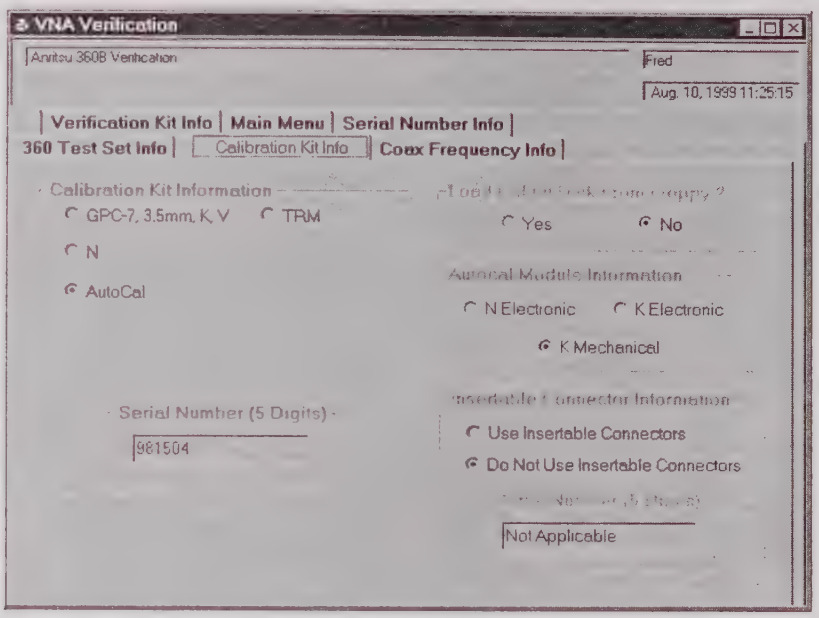
After you make a selection, the program continues in this fashion until enough information has been entered to perform a calibration. At that point, the "Calibrate VNA" button will be enabled so you can start the actual calibration of the VNA. You will have a chance to confirm the information that was input before proceeding with the calibration. Also, at any time up until the confirmation of the information input, You can go back to any stage of the setup and change items you wish to change.

Please bear in mind that changing some choices may cause some of the information to have to be re-entered. For example, if you select a different calibration kit, you will also have to choose the verification kit as well as the frequency range again since the newest selections may not be valid for the previous information that was entered.

If the program found a 360 Series VNA, the program will first prompt you to input the test set's model number.



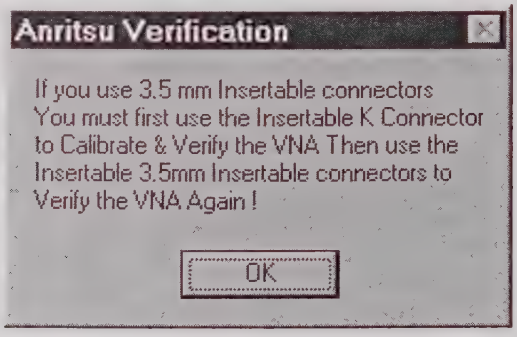

Next, you will enter the information about the calibration kit. The calibration kit coefficients disk should be loaded into the VNA. The tight tolerances of this verification program will almost guarantee the VNA WILL NOT PASS IF THIS IS NOT DONE. The calibration kit disk is not an absolute necessity for the program to run.




In the picture above, a setup was picked to allow the filling in of the maximum amount of information. If you do not pick an 'AutoCal' calibration, then the two boxes labeled "AutoCal Module Information" and "Insertable Connector Information" would be disabled to help prevent errors.

To increase the probability of passing the verification, it is recommended that the calibration kit coefficients disk be loaded into the VNA. (The "No" button is a forced condition in this picture because AutoCal does not have such a disk.) Also, if you move the mouse cursor over a section that has been completed, the message: "This Section is complete. Go to another Red Section" will be displayed informing you that everything is OK so far. You may select another item in a "completed" section at any time but, since some choices may or may not be valid for the new selection, there may be other items that have to be redone.

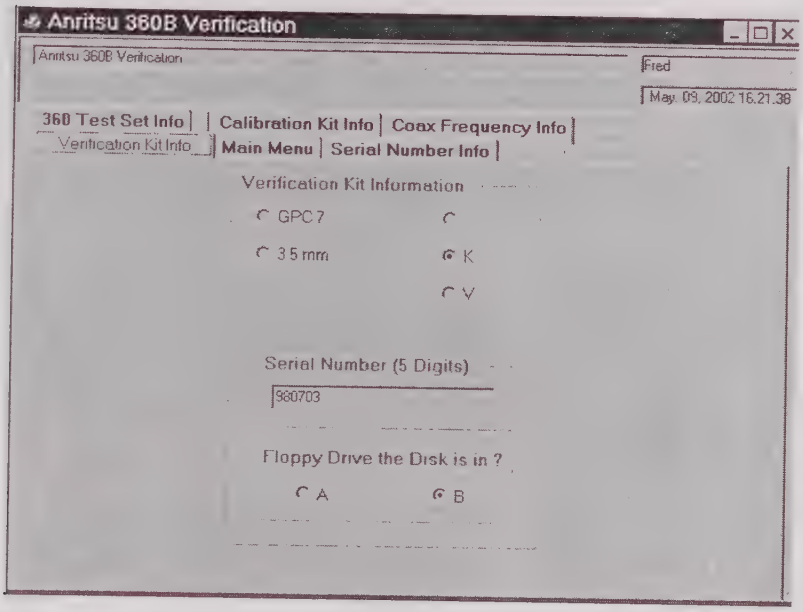
Also, there is an informational note displayed about using the insertable connectors with the AutoCal module.


Anritsu Verification
If you use 3.5 mm Insertable connectors
You must first use the Insertable K Connector
to Calibrate & Verify the VNA Then use the
Insertable 3.5mm Insertable connectors to
Verify the VNA Again !
OK

Once you have entered the required information (at a minimum a calibration kit, the calibration kit serial number, and the calibration kit disk) the program will proceed to the next step, which is gathering the verification kit information.

Some items will be disabled depending on the choices that were made in earlier menus.

Pick the verification kit type, enter the verification kit serial number, and select the floppy drive that the verification kit disk is in.

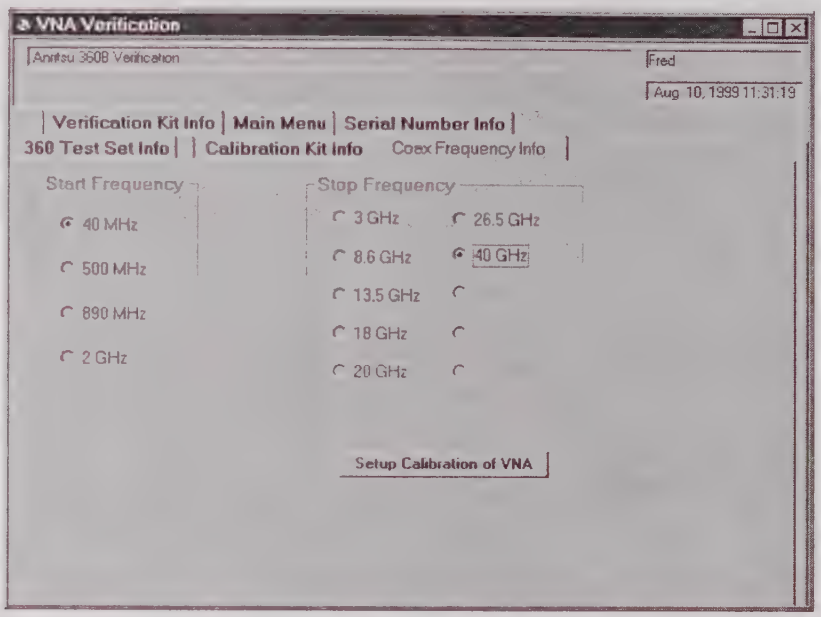



The program will tell you to insert the disk into the disk drive, then check to see if the correct disk (a Version 2 disk) is in the floppy drive.

***Note***

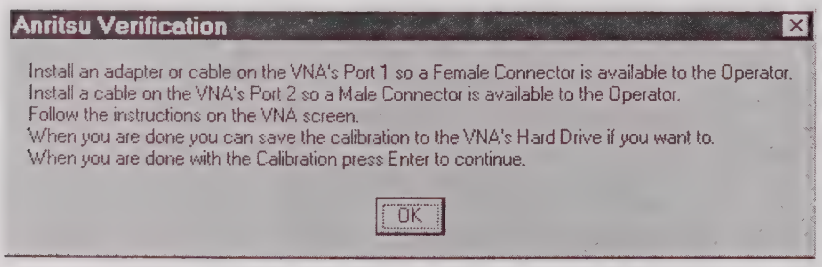
This program WILL NOT WORK with an older Version 1 disk because the tolerances on the Version 1 disk do not conform to the new specifications. If you do not have a Version 2 verification kit disk, you cannot use this program to verify a VNA. Customers that wish to have their verification kit upgraded to Version 2 should contact their local Anritsu customer service center for more information.

The next item that must be entered is the frequency range for the verification to be done. Once a start and stop frequency have been selected, the "Setup Calibration of VNA" button will be enabled.




When you click "Setup Calibration of VNA," you will be asked to confirm if the information entered was correct. If you select No, the program will return to the setup menus so that you can check or change items.

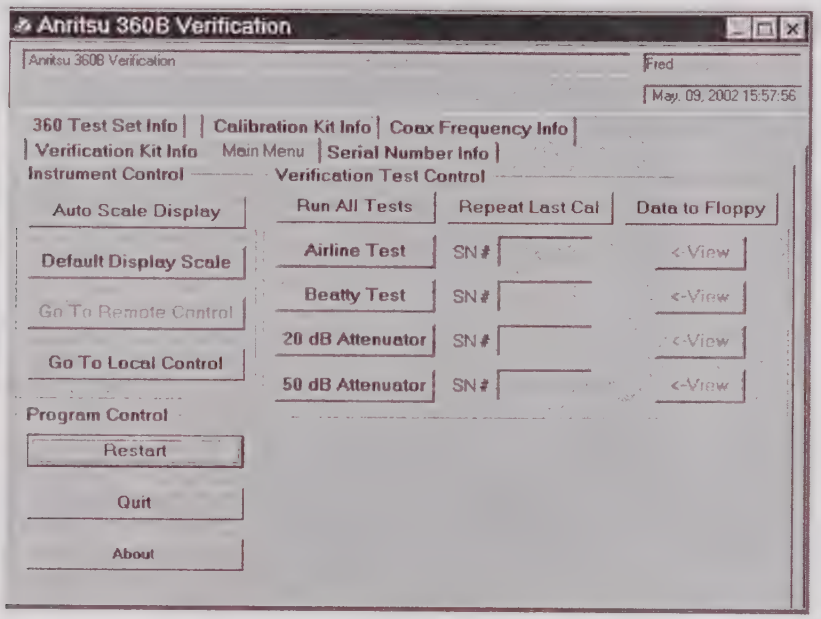
If you select the Yes option, the program will setup the VNA according to the input you supplied. You will be instructed to follow the instructions on the VNA's screen by a dialog box similar to the one shown below.


Anritsu Verification
Install an adapter or cable on the VNA's Port 1 so a Female Connector is available to the Operator.
Install a cable on the VNA's Port 2 so a Male Connector is available to the Operator.
Follow the instructions on the VNA screen.
When you are done you can save the calibration to the VNA's Hard Drive if you want to.
When you are done with the Calibration press Enter to continue.
OK

If the calibration kit chosen was the AutoCal module, then you will see the following text in a dialog box with a scroll bar:

> Please wait for the VNA to reset and setup the calibration. When it is ready, Press Alt & Escape to temporarily exit this program so you can run the AutoCal Program. Or if you want to view these instructions as you setup the AutoCal Program shrink this window so you can view the instructions and the AutoCal Program.
>
> - Important Note -
> If the verification to be performed involves the use of an Insertable Connector the VNA MUST BE CALIBRATED WITH THE INSERTABLE K CONNECTOR INSTALLED ON THE AUTOCAL MODULE. Then replace the Insertable K Connector with the Insertable Connector of your choice for the verification.
>
> After the AutoCal Program is finished you can SAVE the calibration. Also, after the AutoCal Program is finished you should exit the AutoCal program before you continue. Failure to do so may cause unexpected results !!
>
> Choose the Following Settings in the System Options Dialog :
> Set the Analyzer's GPIB Address to the address displayed above.
> Calibrator's Serial Port - The COM port it is connected to the VNA
> is an Anritsu 37000 model then set Analyzer type to Anritsu 37000
> If the VNA is a Anritsu 360 model then set Analyzer type to Anritsu 360 VNA Measurement Averaging Factor - Use Value in VNA
> Video IF BW - Default Value
>
> Choose the following settings in the Setup Dialog :
> type of Calibration - Full 2-Port
> type of Thur - Calibrator or True. {True will give better results.}
> Assurance - Off Isolation Averaging - Off
> Isolation Averaging - No Isolation
>
> If you are using a Anritsu AutoCal Module 36581NNF or a 36581KKF then set the switch averaging to 1.
>
> If you are using a Anritsu AutoCal Module 36582KKF then set the switch averaging to 2.
>
> Note : the sex of the connectors on the AutoCal modules 36581NNF and 36582KKF are reversed compared to the 'Normal' way connections are made. Therefore, connect the AutoCal Module's male connector to the VNA's Port 1.
> Connect the AutoCal Module's female connector to the VNA's Port 2.
> Set the Port Configuration - L = Port 2, R = Port 1
>
> otherwise for the AutoCal Module 36581KKF:
> Set the Port Configuration - L=Port 1, R=Port 2

When you click the OK button in the 'Setup Instructions' dialog box, the program will setup the VNA for running the tests on the verification devices and display the 'Main Menu' shown below.




Program initialization is now complete.

# Chapter 5
# Running the Program

**Contents**

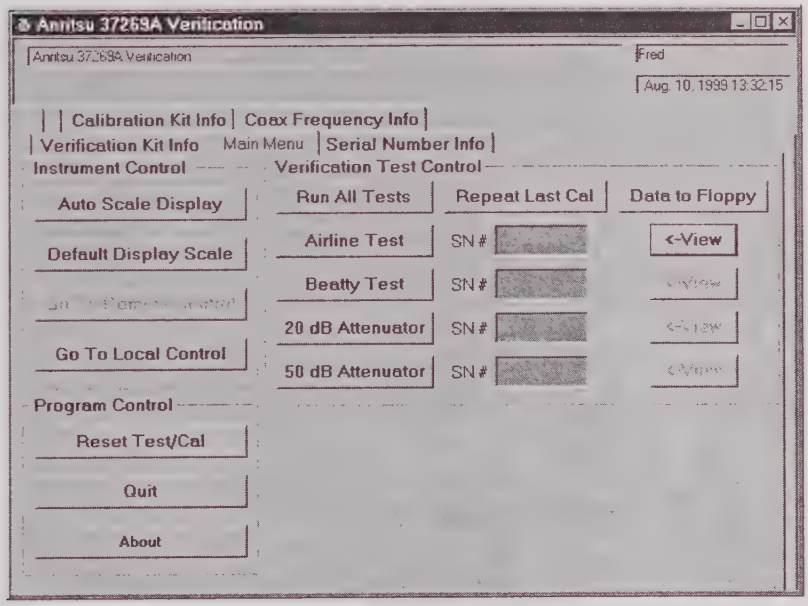

| Paragraph | | Page |
|---|---|---|
| 19 | Running the Program | 17 |
| 20 | Commands | 18 |
| 21 | Running a Test | 20 |


**19**

## Running the Program

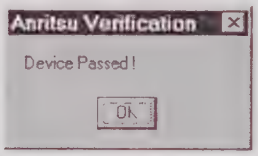
Anytime the program is executing a command from the main menu, the buttons will be disabled until the currently executing command is finished. This is necessary due to the event driven nature of Windows. Also, while a command is being executed, informational messages may be displayed on the screen.

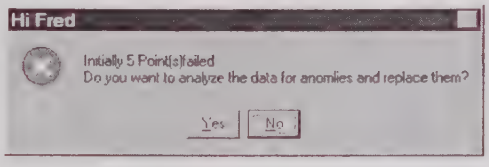
The picture below shows that only the Airline test has been run so far.




The 50 dB Attenuator test has not yet been run. If a device passes, the serial number text will turn GREEN. If a device fails, the serial number text will turn RED. If a test for a device was canceled before pass-fail status could be established, the serial number text will be BLACK. If a device has not been tested there will be no entry for the serial number. Also, if a 'V' verification kit was chosen earlier, the 50 dB attenuator button would say "40 dB Attenuator."

The test results, pass or fail, will be displayed in dialog boxes and in the 'Verification Test Control' frame.

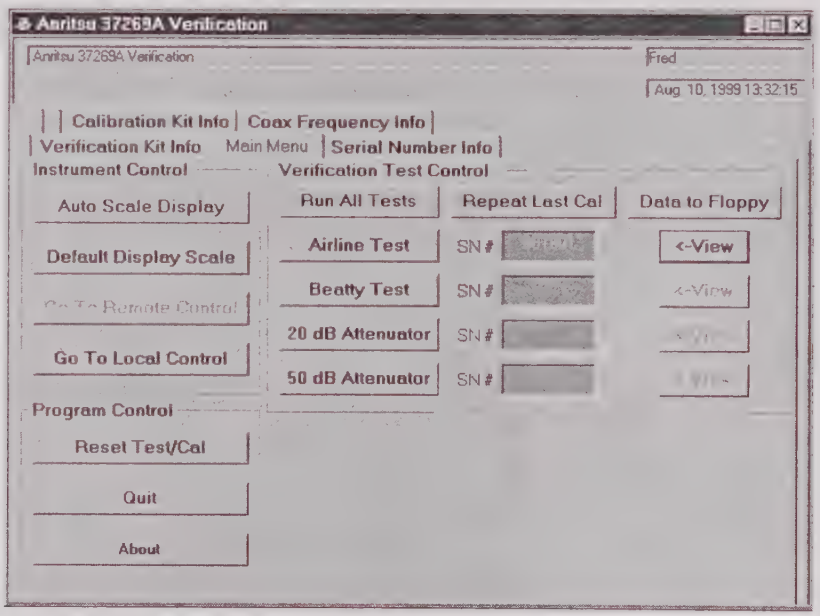



20

## Commands

The Main Menu consists of three frames: Program Control, Instrument Control, and Verification Test Control. Each frame contains command buttons to control various program operations.




### Program Control Frame

#### About

Displays version information, Copyright and other legal notices as well as company contact information.

#### Quit

Selecting Quit will bring up a confirmation box. Selecting Yes will exit the program; selecting No will return the user to the previous screen.

#### Reset Test/Cal

This command allows the operator to change the VNA to test, the frequency range, or the selected verification kit. If you want to change the VNA, frequency range, or verification kit type, the program will reinitialize back to the beginning. If you want to use another like verification kit, the program will re-initialize to the point after calibration.

### Instrument Control Frame

#### Auto Scale Display

This command will automatically scale each channel on the VNA. It is the same as selecting a front panel channel button, then pushing the front panel Auto Scale button for each channel.

*NOTE*

When the program detects the VNA has finished a sweep, the program will auto scale all four channels before continuing.

#### Default Scale Display

This command sets all four channels to a scale of 15 (dB or Unit/Div for a 37XXXX) or 30 (dB or Unit/Div for a 360X) and the reference value to 0. This will allow you to see if the device is properly connected.

#### Go to Remote Control

This command is only available after you have clicked the 'Go to Local Control' button. When you push this button, the program takes control of the VNA and restores the VNA to the same state it was in after the instrument was calibrated.

#### Go to Local Control

This command allows you access to the front panel buttons while the program is running. The instrument is in 'Local Lock Out' unless this button is pushed. This prevents an inadvertent front panel button actuation from affecting the proper operation of the program.

### Verification Test Control Frame

#### Run All Tests

This command button will run all of the tests (Airline, Beatty, 20 dB, 40 to 50 dB) in order. You will be prompted for information as required.

#### Airline Test

This command button will run an airline test only, then display the results.

#### Beatty Test

This command button will run a Beatty airline test only, then display the results.

#### 20 dB Attenuator

This command button will run a 20 dB attenuator test only, then display the results.

#### 40-50 dB Attenuator

This command button will run a 40 or 50 dB attenuator test only, then display the results.

#### Data to Floppy

This command button will write the data files of the last set of tests that were run to the same floppy disk drive that the verification kit disk is in. You will be prompted to remove and reinsert the verification kit disk at the proper times. The program will not write data to the verification kit disk, even if the disk is not write protected.

**Repeat Calibration**
This command button will recalibrate the VNA according to the CURRENT calibration. This provides a way to quickly recalibrate the VNA without having to reset the program parameters in case the original calibration was flawed for some reason.

**View Buttons**
These buttons allow you to view or print the test results without the use of an external program.

21

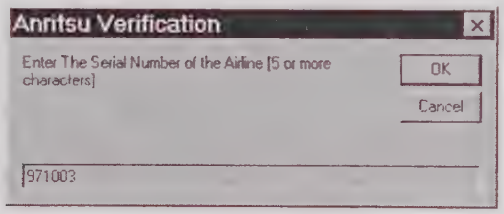
## Running a Test

This section presents the typical test scenario.

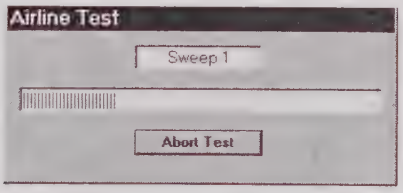
***Note***

> In this section the testing of a Beatty airline is used as an example. If any other device is tested, the program will respond in a similar manner except the word ' Beatty Airline' will be replaced with 'Airline', '20 dB Attenuator', or '50 dB Attenuator' as appropriate.

When either the Run All Tests, Airline Test, Beatty Test, 20 dB Attenuator, or the 40-50 dB Attenuator command button is pushed, the program can respond in one of two ways. If no device has previously been tested, the program prompts you for the serial number of the device to be tested.

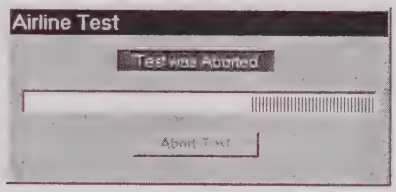



While a test is running, the following dialog box will be displayed:




As the test progresses, vertical bars will be inserted, from left to right, into the progress bar. At the end of the first sweep, the program will display a "Paused" dialog box. The trace display is autoscaled on the VNA so that you can see how the device is doing. During the second sweep, the program will insert vertical bars, from right to left, into the "Sweep2" dialog box. At the end of the second sweep, the program will autoscale the VNA display again.

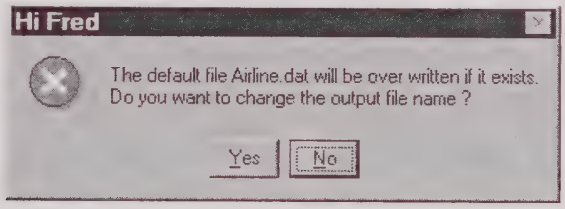
If you abort the test during the first or second sweep, the program will display an informational "Test Aborted" dialog box.




The VNA will abort the current sweep then return to the "Main Menu."

When the test is finished, the program will get the test data from the VNA, read in the data from the verification kit disk, calculate the uncertainties, and inform you if the device passed or failed. If the device failed, the program will display the number of points that failed the test and prompt you to retest the specific failed points.

Please bear in mind that the larger the number of failed points, the longer it will take to recheck them. If there is a large number of failed points, then rechecking those points might be skipped; there is probably something else wrong such as bad or worn connectors or devices. After this option, the program then writes the measurements to the data files. When the program starts to save the data to a file, the program will display the following dialog box.




Select Yes to enter a specific filename to save the data to. Selecting No will cause the program to write the data to the default file name for the device under test. After saving the data, the program will return to the main menu.

# Chapter 6
# Troubleshooting

Contents


| Paragraph | | Page |
|---|---|---|
| 22 | Difficulty Running the Program | 23 |
| 23 | Difficulty Meeting System Specifications | 24 |


22

## Difficulty Running the Program

If you have difficulty getting the program to run properly:

1. Check your GPIB interconnection cables and addresses. For a 360X VNA the GPIB cable between the computer and instrument should be no longer than two meters.
2. Check to see that the Windows GPIB is present on the boot drive, is properly configured, and passes the National Instruments hardware and software tests.
3. This version of the verification software must be installed with the installation program on disk one. The program will not run if is just copied from the floppy disks to the hard disk.
4. Ensure that, after starting-up the performance verification software, the verification kit data disk (Version 2) is installed in drive A or B and that it contains the following files:

   AIRLINE.S12, AIRLINE.S11, AIRLINE.S21, AIRLINE.S22

   BEATTY.S12, BEATTY.S11, BEATTY.S21, BEATTY.S22

   DB20.S12, DB20.S11, DB20.S21, DB20.S22

   DB4050.S12, DB4050.S11, DB4050.S21, DB4050.S22
5. If you are using a 360X VNA, check that the GPIB settings for the GPIB card and the instrument address are correct. The default instrument address is six. Setup both the GPIB card and the instrument according to Appendix B.

If, after checking the above, you are still having difficulty, contact your Anritsu customer service center and ask for the Vector Network Analyzer support engineer for further assistance.

23

## Difficulty Meeting System Specifications

If the verification software appears to run properly, but the results are not within the measurement limits associated with the verification kit:

1. Check both the verification kit and calibration kit devices for signs of physical damage. Make sure that the connectors are clean.
2. Ensure that the serial number of the verification kit data disk matches that shown on the verification kit, and that the verification kit disk is a Version 2 disk.
3. Repeat the process with a fresh calibration. Save the results of both measurements as an aid in troubleshooting, if you require factory assistance.
4. When installing calibration devices, and when measuring verification devices, pay particular attention to proper connector alignment and torque. Torque the connector using the torque wrench supplied with the calibration kit.

If, after following the above steps, you still have difficulty, please contact Anritsu Customer Service at (408) 778-2000 (FAX: (408) 778-0239) and ask for the Vector Network Analyzer Support Engineer for further assistance.

# Appendix A
# Example of Tabular Test Results

Anritsu VNA Verification Version 3.00

VNA Model : 360B  VNA Serial Number : 981501
Test Set Model Number : 3621 A  Test Set Serial Number : 981503
Source Model Number: 360ss69  Source Serial Number : 981502
Calibration Kit Model Number : 3652-1  Calibration Kit Serial Number : 981401
Verification Kit Model Number : 3668  Verification Kit Serial Number : 981402
Date :8/19/99 11:52:51 AM  Operator : Fred
Airline Serial Number : 981301

| | S21 Magnitude | | | | | S21 Phase | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Freq GHz | STD (dB) | MEAS (dB) | DIFF S-M | UNC +/- | Pass Fail | STD DEG | MEAS DEG | DIFF S-M | UNC +/- | Pass Fail |
| .04 | -.0072 | -.0013 | -.0059 | .2400 | | -.7279 | -.7375 | .0096 | 1.9160 | |
| 1.00 | -.0150 | -.0150 | .0000 | .2411 | | -19.0717 | -19.0992 | .0275 | 2.3000 | |
| 2.00 | -.0270 | -.0119 | -.0151 | .2422 | | -38.1178 | -38.1874 | .0696 | 2.7000 | |
| 3.00 | -.0230 | -.0161 | -.0069 | .2433 | | -57.1481 | -57.2633 | .1152 | 3.1000 | |
| 4.00 | -.0207 | -.0175 | -.0031 | .2444 | | -76.2193 | -76.2933 | .0740 | 3.5000 | |
| 5.00 | -.0245 | -.0227 | -.0018 | .2455 | | -95.2885 | -95.3479 | .0594 | 3.9000 | |
| 6.00 | -.0244 | -.0214 | -.0030 | .2466 | | -114.3624 | -114.3997 | .0373 | 4.3000 | |
| 7.00 | -.0390 | -.0261 | -.0129 | .2477 | | -133.4413 | -133.5391 | .0978 | 4.7000 | |
| 8.00 | -.0323 | -.0354 | .0030 | .2488 | | -152.4128 | -152.5198 | .1070 | 5.1000 | |
| 9.00 | -.0259 | -.0270 | .0010 | .2499 | | -171.4536 | -171.5839 | .1302 | 5.5000 | |
| 10.00 | -.0330 | -.0268 | -.0062 | .2510 | | 169.5806 | 169.3428 | .2378 | 5.9000 | |
| 11.00 | -.0311 | -.0255 | -.0055 | .2521 | | 150.4675 | 150.3231 | .1445 | 6.3000 | |
| 12.00 | -.0270 | -.0299 | .0028 | .2532 | | 131.5260 | 131.2803 | .2456 | 6.7000 | |
| 13.00 | -.0414 | -.0366 | -.0048 | .2543 | | 112.3815 | 112.0439 | .3376 | 7.1000 | |
| 14.00 | -.0797 | -.0774 | -.0023 | .2554 | | 93.2610 | 92.9081 | .3529 | 7.5000 | |
| 15.00 | -.0755 | -.0685 | -.0070 | .2565 | | 74.5050 | 74.1548 | .3501 | 7.9000 | |
| 16.00 | -.0534 | -.0523 | -.0011 | .2576 | | 55.7022 | 55.2081 | .4941 | 8.3000 | |
| 17.00 | -.0356 | -.0394 | .0039 | .2587 | | 36.5156 | 36.0877 | .4280 | 8.7000 | |
| 18.00 | -.0140 | -.0192 | .0053 | .2598 | | 17.1942 | 16.8801 | .3141 | 9.1000 | |
| 19.00 | -.0301 | -.0331 | .0030 | .2609 | | -1.8969 | -2.2218 | .3249 | 9.5000 | |
| 20.00 | -.0377 | -.0381 | .0004 | .2620 | | -20.8544 | -21.2927 | .4383 | 9.9000 | |
| 21.00 | -.0541 | -.0499 | -.0041 | .2631 | | -39.8890 | -40.1863 | .2973 | 10.3000 | |
| 22.00 | -.0542 | -.0536 | -.0006 | .2642 | | -59.0083 | -59.4669 | .4586 | 10.7000 | |
| 23.00 | -.0338 | -.0360 | .0023 | .2653 | | -78.0750 | -78.6411 | .5661 | 11.1000 | |
| 24.00 | -.0427 | -.0286 | -.0141 | .2664 | | -96.9958 | -97.4680 | .4722 | 11.5000 | |
| 25.00 | -.0556 | -.0405 | -.0151 | .2675 | | -116.0769 | -116.5969 | .5200 | 11.9000 | |
| 26.00 | -.0495 | -.0506 | .0012 | .2686 | | -135.1926 | -135.7708 | .5782 | 12.3000 | |
| 27.00 | -.0524 | -.0535 | .0010 | .2697 | | -154.2416 | -154.8237 | .5820 | 12.7000 | |
| 28.00 | -.0618 | -.0494 | -.0124 | .2708 | | -173.3450 | -173.8467 | .5017 | 13.1000 | |
| 29.00 | -.0709 | -.0586 | -.0123 | .2719 | | 167.6730 | 167.0468 | .6262 | 13.5000 | |
| 30.00 | -.0615 | -.0557 | -.0058 | .2730 | | 148.6410 | 148.0708 | .5702 | 13.9000 | |
| 31.00 | -.0670 | -.0626 | -.0044 | .2741 | | 129.6169 | 129.1705 | .4464 | 14.3000 | |
| 32.00 | -.0561 | -.0382 | -.0179 | .2752 | | 110.4867 | 110.0088 | .4779 | 14.7000 | |
| 33.00 | -.0867 | -.0185 | -.0682 | .2763 | | 91.3969 | 90.6197 | .7772 | 15.1000 | |
| 34.00 | -.0759 | -.0628 | -.0131 | .2774 | | 72.4525 | 71.6582 | .7943 | 15.5000 | |
| 35.00 | -.0564 | -.0762 | .0198 | .2785 | | 53.4577 | 52.7349 | .7228 | 15.9000 | |
| 36.00 | -.0693 | -.0683 | -.0010 | .2796 | | 34.2709 | 33.6507 | .6203 | 16.3000 | |
| 37.00 | -.0811 | -.0679 | -.0132 | .2807 | | 15.2775 | 14.4831 | .7945 | 16.7000 | |
| 38.00 | -.0883 | -.0648 | -.0235 | .2818 | | -3.9279 | -4.6249 | .6971 | 17.1000 | |
| 39.00 | -.1384 | -.0934 | -.0450 | .2829 | | -23.2664 | -24.0578 | .7914 | 17.5000 | |
| 40.00 | -.1644 | -.1409 | -.0235 | .2840 | | -41.9571 | -42.9153 | .9582 | 17.9000 | |

# Appendix B
# GPIB Card and Instrument Settings

Following are the recommended GPIB Card and Instrument Settings

**GPIB Board Settings**

Primary Address = 0
Secondary Address = NONE or 0
Timeout Setting = 10 seconds

Terminate Read on EOS = no or unchecked
Set EOI with EOS on Writes = yes or checked
Type of compare on EOS = 8-bit
EOS Byte = 0Ah or decimal 10
Send EOI at end of Write = yes or checked

System Controller = yes or checked
Assert REN when SC = yes or checked
Enable Auto Serial Polling = No or unchecked
Enable CIC protocol = No or unchecked
Bus Timing = 2 µseconds
Parallel Poll Duration = Default

The following settings may vary depending on the GPIB Card type and Operating System selected.

Use this GPIB Interface = yes or checked
Board Type = your board type (PCIIA, PCI, etc.)
Base I/O Address = consult the GPIB card manual
DMA Channel = consult the GPIB card manual
Interrupt Level = consult the GPIB card manual

**Instrument Settings**

Primary GPIB Address = 6
Secondary GPIB Address = NONE
Timeout Setting = 10 seconds
Serial Poll Timeout = 1 second

Terminate Read on EOS = no or unchecked
Set EOI on EOS on Writes = yes or checked
Type of compare on EOS = 8-bit
EOS Byte = 0Ah or decimal 10
Send EOI at end of Write = yes or checked

Enable Repeat Addressing = no or unchecked

# Appendix C
# Allowable Calibration Kit VNA, Verification Kit Combinations

This set of tables is to be used as a guide in determining if you can perform verifications on an instrument with a given calibration and verification kit. There are three sets of verification kit tables and three sets of calibration kit tables. The verification kit tables cross-reference verification kits with VNA's. There is one table set for 37000 series VNA's, MS462XX VNMS's, and one table for 360X VNA's. The table for 360X VNA's is further broken down into like test set groupings. Each calibration kit has been assigned a Reference Code. This Reference Code is also in the verification kit tables.

One way to use the charts is to start with a verification kit chart. Pick the instrument-test set to be used in the test from the far-left column. Next pick the verification kit to be used in the test from the top row. Scan to the box where the instrument-test set and verification kit intersects. If there is a reference code for a calibration kit in that box then the combination of equipment picked can be verified. If there is not a reference code in that box then the combination of equipment picked can not be verified.

**Table C-1.** Allowable Calibration Kit - Verification Kit - Instrument Combinations (1 of 3)

| | Coax **Verification Kit** | | | | | |
|---|---|---|---|---|---|---|
| **A, B, or C Models** | **N (3663)** | **3.5 mm (3666)** | **GPC7 (3667)** | **K (3668)** | **V (3669)** | **V (3669B)** |
| 37147 | | | | A3* | | |
| 37169 | | | | A3* | | |
| 37(2/3)11 | A4, B1 | A1, B4, B5 | A2 | A3, B2, B4 | | |
| 37(2/3)17 | A4, B1 | A1, B4, B5 | A2 | A3, B2, B4 | | |
| 37(2/3)25 | A4, B1 | A1, B4, B5 | A2 | A3, B2, B3, B6, B7 | | |
| 37(2/3)47 | A4, B1 | A1, B4, B5 | A2 | A3, B2, B3, B6, B7 | | |
| 37(2/3)69 | A4, B1 | A1, B4, B5 | A2 | A3, B2, B3, B6, B7 | | |
| 37(2/3)77 | | | | A3 | A5 | A5 |
| 37(2/3)97 | A4 | A1 | A2 | A3 | A5 | A5 |

**Table C-1.** Allowable Calibration Kit - Verification Kit - Instrument Combinations (2 of 3)

| Coax Verification Kit | | | | | | |
|---|---|---|---|---|---|---|
| **360, 360A 360B Test Sets** | **N (3663)** | **3.5 mm (3666)** | **GPC7 (3667)** | **K (3668)** | **V (3669)** | **V (3669B)** |
| 3610, 3620 | A4, B1 | A1, B4, B5 | A2 | A3, B2, B6, B7 | | |
| 3611, 3621 | A4, B1 | A1, B4, B5 | A2 | A3, B2, B6, B7 | | |
| 3612, 3622 | | | | A3 | A5 | A5 |
| 3613, 3623 | A4 | A1 | A2 | A3 | A5 | A5 |
| 3630 | | | | | | |

| Coax Verification Kit | | | | | | |
|---|---|---|---|---|---|---|
| **A** or B*** Models** | **N (3663LF)** | **3.5 mm (3666LF)** | **GPC7 (3667LF)** | **3750R (3.5 mm)** | **3751R-1 (GPC7)** | **3753R (N)** |
| MS462(2/3) (to 6 GHz) | C3 | C1 | C2 | E1 | E2 | E3 |
| 8 GHz Units | | | | E1 | E2 | E3 |

| Millimeter Wave Verification Kit | | | | | | |
|---|---|---|---|---|---|---|
| **A or C Models** | **3655Q (WR-22)** | **3655V (WR-15)** | **3655E (WR-12)** | **3655EE (WR-12E)** | **3655W (WR-10)** | **3655WE (WR-10E)** |
| 37147 | D1 | D2 | D3 | D3 | D4 | D4 |
| 37169 | D1 | D2 | D3 | D3 | D4 | D4 |

| Coax Calibration Kit | | | | | | |
|---|---|---|---|---|---|---|
| | **3650-1 (3.5 mm)** | **3651-1 (GPC7)** | **3652-1 (K)** | **3653 (N)** | **3654 (V)** | **36581NNF (N AutoCal)** |
| Reference Code | A1 | A2 | A3 | A4 | A5 | B1 |

| Coax Calibration Kit | | | | | | |
|---|---|---|---|---|---|---|
| | **36581KKF (K Electronic AutoCal 20 GHz)** | **36582KKF (K Mechani-cal AutoCal 40 GHz)** | **36581KKF with 36583L** | **36582KKF with 36583L** | **36581KKF with 36583K** | **36582KKF with 36583K** |
| Reference Code | B2 | B3 | B4 | B5 | B6 | B7 |

| Coax Calibration Kit | | | | | | |
|---|---|---|---|---|---|---|
| | **3750LF (3.5 mm)** | **3751LF-1 (GPC7)** | **3753LF (N)** | **3750R (3.5 mm)** | **3751R-1 (GPC7)** | **3753R (N)** |
| Reference Code | C1 | C2 | C3 | E1 | E2 | E3 |

**Table C-1.** Allowable Calibration Kit - Verification Kit - Instrument Combinations (3 of 3)

| | Millimeter Wave Calibration Kit | | | | | |
|---|---|---|---|---|---|---|
| | **3655Q (WR-22)** | **3655V (WR-15)** | **3655E (WR-12)** | **3655EE (WR-12E)** | **3655W (WR-10)** | **3655WE (WR-10E)** |
| Reference Code | D1 | D2 | D3 | D3 | D4 | D4 |

Notes:

Option 3 - Asymmetrical test set selection is permitted on 3610, 3611, 3612, 3613 test sets only.

36583L and 36583K are phase equalized insertable adapters.

* Requires the use of a SM5235 or SM5392 S-parameter test set adapter.

** "A" models are restricted to a one-path, two-port calibration.

*** Port 3 Verifications are NOT SUPPORTED for "B" models with Option 6 and an external source.

Anritsu

# *Subject Index*

# *Subject Index*


## *Number*

37397A Source Lock Signal Path Diagram . . . . . 5-26
37397A Test Signal Path Diagram . . . . . 5-25

## *A*

A13 I/O Interface #1 PCB Assembly . . . . . 7-15
A14 I/O Interface #2 PCB Assembly . . . . . 7-15
A15 Graphics Processor PCB Assembly . . . 7-16
A16 Hard Disk PCB Assembly . . . . . 7-16
A17 System Motherboard Assembly . . . . . 7-16
A18 Rear Panel Interface PCB . . . . . 7-17
A18 REAR PANEL PCB . . . . . 8-22 -8 -24
A1-A9 and A13-A16 PCB Assemblies Removal Diagram . . . . . 8-7
A1–A9 AND A13–A16 PCBS . . . . . 8-6
A21A1 Source YIG Bias Control PCB . . . . . 8-32
A21A2 ADJUSTMENT (37397A) . . . . . 6-14 -6 -16
A21A2 Source Control PCB . . . . . 8-31
A24 VME BUS TERMINATOR PCB . . . . . 8-12
A31 Buffer Amplifier/Sampler Assembly . . . 8-28
A41 Power Amplifier Assembly . . . . . 8-27
A5 A/D Converter PCB . . . . . 7-12
A7 PCB, 10 MHz Timebase . . . . . 7-9
A7 PCB, LO3 . . . . . 7-12
A8 ADJUSTMENT (37397A) . . . . . 6-13
A8, Source Lock/ Signal Separation and Control PCB . . . . . 7-11
A9 Main Processor PCB Assembly . . . . . 7-13
A9 PCB BBRAM CHIP . . . . . 8-6 -8 -9
A9 PCB SRAM BATTERY . . . . . 8-10 -8 -11
Acrobat Reader . . . . . 1-3
Adjustments
  A21A2 (37397A) . . . . . 6-14
  A8 (37397A) . . . . . 6-13
  Frequency Calibration . . . . . 6-5
  Internal Hardware Adjustments and Calibratioin . . . . . 1-5
  Introduction to . . . . . 6-3
  LO1 Calibration . . . . . 6-3
  LO2 Calibration . . . . . 6-4
  RF Power/ALC Calibration . . . . . 6-8
  Source Lock Threshold . . . . . 6-11
Adobe Acrobat . . . . . 1-3
ANALOG SUBSYSTEM ASSEMBLIES 7-7 -7 -12
ANRITSU Service Centers . . . . . 1-9,2-4
ASSOCIATED INFORMATION IN THIS MANUAL 5-3
Avoid Mechanical Shock . . . . . C-4
Avoid Over Torquing Connectors . . . . . C-4

## *B*

Boot-up Problems . . . . . 5-7
Boot-up Process Sequence . . . . . 5-7
Buffer Amplifier/ Sampler(A31) . . . . . 8-27

## *C*

CALIBRATION AND MEASUREMENT CONDITIONS . . . . . 4-3
CD ROM . . . . . 1-3
CHECKING THE SERVICE LOG . . . . . 3-4
Connector Maintenance
  Cleaning . . . . . C-4
  INTRODUCTION . . . . . C-3
  Mechanical Shock . . . . . C-4
  Pin Depth Problems . . . . . C-3
  Pin Depth Tolerances . . . . . C-4
  Precautions . . . . . C-3
  Repair/Maintenance . . . . . C-5
  Teflon Tuning Washer . . . . . C-4
  Torque . . . . . C-4
  Visual Inspection . . . . . C-5
Consummsable Parts . . . . . 2-6
COVERS . . . . . 8-4 -8 -5
CRT Display Test Failures: . . . . . 5-21

## *D*

Diagnostic Menus
  INTRODUCTION . . . . . A-3
Diagnostics Menus
  H/W (Hardware) Calibrations . . . . . A-5
  Installed Options . . . . . A-4
  Peripheral Tests . . . . . A-4
  Read Service Log . . . . . A-3
  Start Self Test . . . . . A-3
  Troubleshooting . . . . . A-4
DIAGNOSTICS MENUS . . . . . A-3 -A -6
Diagnostics Menus Flowchart . . . . . A-7
DIGITAL SUBSYSTEM ASSEMBLIES 7-13 -7 -15
DigitalSubsystem Block Diagram . . . . . 7-14
DISK RELATED ERROR MESSAGES . . . . B-3
Down Converter Assembly . . . . . 8-33

## E

Electro-static discharge procedures . . . . . 1-9
EQUIPMENT REQUIRED . . . . . 8-3
Error Code DE Lock Failure Troubleshooting 5-14
Error Codes . . . . . 5-10
Error Messages
Disk Related . . . . . B-3
Disk Related Error Messages . . . . . B-3
GPIB Related . . . . . B-3
INTRODUCTION . . . . . B-3
Operational Error Messages . . . . . B-3
Service Log . . . . . B-3
EXCHANGE ASSEMBLY PROGRAM . . . . . 2-3
Exploded View of 372XXB Chassis Covers . . 8-5
External Keyboard Interface Test . . . . . 3-7

## F

Factory Repairable Non-Exchange Parts . . . 2-6
Failed Assembly Exchange Program . . . . . 1-8
FAN ASSEMBLY . . . . . 8-21
Field Service Kits . . . . . 1-7
FLOPPY DISK DRIVE . . . . . 8-17 -8 -18
Floppy Disk Drive Assembly . . . . . 7-16
Floppy Disk Problems . . . . . 5-9
FREQUENCY CALIBRATION . . . . . 6-5 -6 -7
Front Panel Assembly . . . . . 7-16
FRONT PANEL ASSEMBLY . . . . . 8-12 -8 -13
Front Panel Test . . . . . 3-7
Front Panel Test Failures . . . . . 5-22
Functional Assembly Level Troubleshooting . . 1-5

## G

GPIB Interface Test . . . . . 3-9
GPIB Interface Test Failures . . . . . 5-22
GPIB Related Error Messages . . . . . B-3
GPIB RELATED ERROR MESSAGES . . . . B-3

## H

H/W Calibrations . . . . . A-5
Hard Disk Problem 1 . . . . . 5-8
Hard Disk Problem 2 . . . . . 5-9
Hard Disk Problems . . . . . 5-8

## I

IDENTIFICATION NUMBER . . . . . 1-3
IF Section . . . . . 7-11
Input Coupler(s)/ Low Freq Bridge(s) . . . . . 8-26
Installed Options . . . . . A-4
Internal Hardware Adjustments and Calibration . . . . . 1-5
Internal VGA Monitor . . . . . 7-19
Isolation Procedures, Troubleshooting . . . . 5-19

## K

Keep Connectors Clean . . . . . C-4
KEY SYSTEM PARAMETERS . . . . . 4-6 -4 -7

## L

LCD BACKLIGHT LAMP . . . . . 8-17
LCD Test . . . . . 3-6
Line Source and Interface Checks . . . . . 5-4
LIQUID CRYSTAL DISPLAY (LCD) . . . . . 8-16
LO 2 CALIBRATION . . . . . 6-4
LO1 CALIBRATION . . . . . 6-3
Location of BBRAM Chip on the A9 PCB . . . 8-9
Location of Floppy Disk Drive Assembly Mounting Plate Screws . . . . . 8-18
Location of Internal LCD Assembly Mounting Screws . . . . . 8-16
Location of Internal VGA Monitor Assembly Mounting Screws . . . . . 8-15
Location of Mounting Screws for Rear Panel Assemblies . . . . . 8-19
Location of SRAM Battery on the A9 PCB . . 8-11
Location of the A24 VME Bus Terminator PCB Assembly . . . . . 8-12

## M

MAIN CHASSIS ASSEMBLIES . . . . 7-16 -7 -19
Major Assemblies Location Diagram (Bottom View) (Not 37397A) . . . . . 2-8 -2 -9
Major Assemblies Location Diagram (Top View) . . . . . 2-7
MANUAL SCOPE . . . . . 1-3
MEASUREMENT ACCURACY . . . . . 4-4
Measurement Conditions Check List . . . . . 5-23
Measurement Environment Considerations . . 4-6
MEASUREMENT IN QUESTION . . . 5-22 -5 -24
Measurement Technique . . . . . 4-7
Miscellaneous /Integrated Assemblies . . . . . 2-6

## O

ONLINE MANUAL . . . . . 1-3
Operational Error Messages . . . . . B-3
OPERATIONAL ERROR MESSAGES . . . . B-3
Overall Block Digram of 373XXA VNA System 7-5

## P

PARTS ORDERING INFORMATION . . 2-4 -2 -10
Performance Specifications . . . . . D-1,1-1

PERFORMANCE SPECIFICATIONS · · · · · 1-9
Performance Verification Software · · · · · · 1-4
Peripheral Tests · · · · · · · · · · · · · · · · A-4
PERIPHERALS AND INTERFACES · · 3-6 -3 -9
PERIPHERALS/ INTERFACE · · · · · · · · 5-21
Phase Lock Error Codes (6000 Series) · · · · 5-11
Pin Depth
Problems · · · · · · · · · · · · · · · · · · C-3
Tolerances · · · · · · · · · · · · · · · · · C-4
Pin-Depth Tolerance · · · · · · · · · · · · · C-4
Power Amplifier · · · · · · · · · · · · · · · 8-26
Power Supply Module · · · · · · · · · · · · 7-18
POWER SUPPLY MODULE · · · · · · · · · 8-21
Power Supply Module Check · · · · · · · · · 5-6
Power Supply Voltages Check · · · · · · · · 5-4
Precautions · · · · · · · · · · · · · · · · · · C-3
PRECAUTIONS · · · · · · · · · · · · · C-3 -C -4
Preventive Service · · · · · · · · · · · · · · 1-6
Printed Circuit Assemblies · · · · · · · · · · 2-5
Printer Interface Test · · · · · · · · · · · · · 3-7
Printer Interface Test Failures · · · · · · · · 5-22

## R

Read Service Log · · · · · · · · · · · · · · · A-3
Rear Panel Assembly · · · · · · · · · · · · 7-17
REAR PANEL ASSEMBLY · · · · · · · 8-19 -8 -20
Receiver Module · · · · · · · · · · · · · · · 7-10
RECOMMENDED TEST EQUIPMENT 1-9 -1 -11
Related Manuals · · · · · · · · · · · · · · · 1-4
RELATED MANUALS · · · · · · · · · · · · · 1-4
Removal of Front Panel Assembly · · · · · · 8-13
Removal of Signal Source Module · · · · · · 8-29
Remove and Replace
A12 VME Bus Terminator PCB · · · · · · 8-12
A13-A16 PCBs · · · · · · · · · · · · · · · · 8-6
A18 Rear Panel PCB · · · · · · · · · · · · 8-22
A1-A9 PCBs · · · · · · · · · · · · · · · · · · 8-6
A9 PCB BBRAM Chip · · · · · · · · · · · · 8-6
A9 PCB SRAM Battery · · · · · · · · · · · 8-10
Covers · · · · · · · · · · · · · · · · · · · · · 8-4
Equipment Required · · · · · · · · · · · · · 8-3
Fan Assembly · · · · · · · · · · · · · · · · 8-21
Floppy Disk Drive · · · · · · · · · · · · · · 8-17
Front Panel Assembly · · · · · · · · · · · · 8-12
INTRODUCTION · · · · · · · · · · · · · · · 8-3
LCD · · · · · · · · · · · · · · · · · · · · · · · 8-16
LCD Backlight Assembly · · · · · · · · · · 8-17
Power Supply Module · · · · · · · · · · · · 8-21
Rear Panel Assembly · · · · · · · · · · · · 8-19
Signal Source Modules · · · · · · · · · · · 8-29
Test Set Modules · · · · · · · · · · · · · · 8-25
VGA Display Monitor · · · · · · · · · · · · 8-14
REPAIR/ MAINTENANCE · · · · · · · · · · C-5
REPLACEABLE SUBASSEMBLIES AND PARTS · · · · · · · · · · · · · · · · · · · · · · 2-3
RF POWER/ALC CALIBRATION · · · · 6-8 -6 -10
RF Power/ALC Calibration Adjustment · · · · 6-8

## S

Scope of Manual · · · · · · · · · · · · · · · · 1-3
Screen Display Problems · · · · · · · · · · 5-10
Self Test · · · · · · · · · · · · · · · · · · · · 3-5
SELF TEST · · · · · · · · · · · · · · · · · · · 3-5
Self TestError Codes · · · · · · · · · · · · · 5-11
SERVICE CENTERS · · · · · · · · · · · · · 1-9
service log · · · · · · · · · · · · · · · · · · · B-3
Service Log · · · · · · · · · · · · · · 3-3 -3 -4,5-12
Service Log Error Messages · · · · · · · · · B-3
Service Log Snap Shot Data · · · · · · · · · 5-12
Service Software · · · · · · · · · · · · · · · 1-7
SERVICE STRATEGY · · · · · · · · · · · · 1-5
SERVICE SUPPORT · · · · · · · · · · · 1-6 -1 -8
Servicing Specially Modified Instruments · · · 1-6
SIGNAL PATH · · · · · · · · · · · · · · · · 3-10
Signal Source Module · · · · · · · · · · · · 7-7
Signal Source Module RF/Microwave Components · · · · · · · · · · · · · · · · · · 2-6
Signal Source Parts Location Diagram · · · · 2-10
Signal Source Phase Lock Loop Assemblies · 5-17
Signal Source Problems · · · · · · · · · · · 5-17
Signal Source/Test Set Module Error · · · · · 5-18
Signal Source/Test Set Problems
Introduction to · · · · · · · · · · · · · · · 5-18
SOURCE LOCK THRESHOLD · · · · 6-11 -6 -12
SOURCE/TEST SET/RECEIVER · · · 5-17 -5 -20
S-parameter · · · · · · · · · · · · · · · · · · 4-3
Special Precautions · · · · · · · · · · · · · 4-4
Specifications, Performance · · · · · · · · · 1-1
Standard Conditions · · · · · · · · · · · · · 4-3
STANDARD OPTIONS · · · · · · · · · · · · 1-4
Start Self Test · · · · · · · · · · · · · · · · · A-3
STATIC SENSITIVE COMPONENT HANDLING PROCEDURES · · · · · · · · · · · · · · · · 1-9
Switched Doubler Module Assembly · · · · · 8-28
Switched Filter Assembly · · · · · · · · · · 8-33
SYSTEM HAS ERROR CODE · · · · · 5-10 -5 -16
System Description
A13 I/O Interface #1 PCB · · · · · · · · · 7-15
A14 I/O Interface #2 PCB · · · · · · · · · 7-15
A15 Graphic Processor PCB · · · · · · · · 7-16

MP MASTER
MA30559